Energy Harvesting Techniques for Autonomous WSNs/RFID with a Focus on RF Energy Harvesting

Vom Fachbereich 18
Elektrotechnik und Informationstechnik
der Technischen Universität Darmstadt
zur Erlangung der Würde eines
Doktor–Ingenieurs (Dr.-Ing.)
genehmigte Dissertation

von

M.Sc.
Ping Zhao
geboren am 06. Dez. 1983
in Shandong, China

Referent:	Prof. Dr. Dr. h. c. mult. Manfred Glesner
Korreferent:	Prof. Dr.-Ing. Thilo Bein
Tag der Einreichung:	23. November 2011
Tag der mündlichen Prüfung:	27. April 2012

D17

Darmstadt 2012

To my dearest husband & daughter
Martin & Cecilia

Acknowledgement

This dissertation is the result of my work as a PhD student, teaching and research assistant at the Microelectronic Systems Research Group at Technischen Universität Darmstadt. Foremost, I would like to sincerely thank my *Doktorvater*, Prof. Manfred Glesner, for his wise guidance and mentoring through my doctorate study and research, and also for his trust with involving me in diverse research projects and teaching activities. His continuous encouragement, patience and support helped me get through many scientific and practical challenges.

I also want to express my gratitude to Prof. Thilo Bein, from Fraunhofer-Institut für Betriebsfestigkeit und Systemzuverlässigkeit LBF, for accepting to act as a second reviewer for this dissertation. His detailed comments and observations have been immensely valuable for improving the quality of this manuscript. Furthermore, I would like to thank Prof. Roland Werthschützky, Prof. Klaus Hofmann and Prof. Hans Eveking for acting as members of the examination committee.

During this work, I have collaborated with many colleagues. I wish to sincerely thank Francois Philipp and Yuliang Zheng for the constructive discussions, excellent advices and practical help, without their support, this work could not have been accomplished smoothly. I am also grateful to all colleagues at the institute with whom I had shared a pleasant time. The kind help and support of Harish Balasubramaniam, Yuan Fang, Ramkumar Ganesan, Ashok Jaiswal, Hans-Peter Keil, Leandro Möller, Jing Ning, Sebastian Pankalla, Faizal Samman, Alex Schnberger, Lufei Shen, Christopher Spies, Pongyupinpanich Surapong and Haoyuan Ying provided an atmosphere of cordiality and friendship at the workplace, where during pregnancy I could concentrate on writing the final manuscript.

In the first years of my doctorate study, I have benefited from the valuable experience shared by my former colleagues Petru -Bogdan Bacinschi, Andre Guntoro, Heiko Hinkelmann, Prof. Thomas Hollstein, Massoud Momeni, Tudor Murgan, Oana Mutihac, Oliver Soffke, and to them, I express my sincere gratitude. Further, I wish to thank the technicians, Roland Brand and Andreas Schmidt, for their help in solving many technical problems. Warm thanks also to dear secretaries, Silvia Hermann and Iselona Klenk for their continuous support in a multitude of administrative issues.

My lovely attitude goes to everybody in the Chinese Bible Study Group in Darmstadt and the Chinese Christian Church in Frankfurt. Those wonderful occasions I will always

cherish, the prayer meetings, the bible studies, the choir practice, the Christmas parties... I am enormously indebted to my parents for all their efforts, love and support, and for the received education and opportunities. Last but not least, I give my loving thanks to my little family. The great love and support from my dear husband Martin has accompanied me over the last five years. His attentive care and consideration of our newborn baby helped me concentrate on preparing for the examination. I thank the Lord for the most precious gift in my life, my little daughter Cecilia, who has accompanied me and kept bringing me so much joy, and through her I learned what love is.

Ilsfeld, 2012

Abstract

Supply circuits that harvest energy from surrounding ambient or dedicated sources have drawn much interest recently for providing a possibility of energy-autonomy to the wireless sensing devices. The objective of this thesis is to optimize the power transfer efficiency of the RF/microwave energy transducers in WSN/RFID applications. For this purpose, analysis on the power utilization of the wireless devices at different working states has been done, which implies a space of improving the power transfer efficiency by employing a novel design concept in the RF/microwave energy transducers.

In order to observe a deep insight of the charge-pump based energy transducer, an analytical derivation has been implemented based on a compact I/V model for MOSFET working in strong inversion and subthreshold regions. The derivation provides a mathematical direction for the impact of the power consumption of the wireless device on the input impedance of the charge-pump rectifier, which acts as a core element in the energy transducer. With expressing the input impedance of the rectifier into a shunt connection of a resistor and a capacitor, as the load current consumption reduces the shunt resistance increases dramatically while the shunt capacitance holds a relatively constant value. This work proposes a methodology of employing an adaptively adjusted matching network between the rectifier and the antenna in order to optimize the power transfer efficiency according to the instant power consumption of the wireless devices on different working states.

For read-only wireless devices with no embedded batteries, like RFID transponders, a tiny storage capacitor of pico-farad which can be charged-up to a certain voltage in microseconds is usually employed as a DC supplier. During the communication between reader and transponder, the reader radiates RF power continuously to supply the transponder. Extra power supply is required to adjust the matching network electrically for optimal power transfer, which raises a new challenge to the batteryless devices. A solution is proposed in this work that an auxiliary rectifier with a smaller constant load current consumption is employed to supply the feedback control circuitries.

Besides, the abovementioned methodology is also applied in charging-up procedure of a wireless device which employs a supercapacitor as its charge storage. The charging-up procedure is extended to hours due to the huge volume of the capacitive storage, and the charging speed becomes a critical issue. During the charging-up, the output voltage of the recti- fier increases exponentially, while the charging current reduces exponentially.

The input impedance derived for steady-state is not precisely applicable yet theoretically directive in this situation. A novel application of adaptively tunable matching network in transient process is implemented to accelerate the charging process of the wireless devices.

Kurzfassung

Schaltungen, die (natürlich vorhandene oder künstlich eingebrachte) Energie aus ihrer Umgebung beziehen und in elektrische Energie umwandeln (“energy harvesting”) haben in jüngerer Zeit grosses Interesse auf sich gezogen. Mit ihnen soll es zukünftig möglich sein, vor allem drahtlose Messgeräte energieautark zu betreiben. Ziel der vorliegenden Arbeit ist die Optimierung von Schaltungen zur Energiegewinnung aus hochfrequenten elektromagnetischen Feldern zur Versorgung von drahtlosen Sensorknoten und RFID-Transpondern. Zu diesem Zweck wurde der Leistungsbedarf verschiedener drahtloser Geräte in verschiedenen Arbeitszuständen analysiert. Diese Analyse zeigt, dass sich die Effizienz der Leistungsbertragung durch neuartige Übertragerschaltungen steigern lässt. Zwecks besseren Verständnisses von Ladungspumpen-basierten Energiewandlern wurde ein analytisches Modell erstellt, dessen Kern eine kompakte Beschreibung der Strom-Spannungs-Kennlinie von MOSFETs in starker Inversion und im Sub-Threshold-Betrieb darstellt. Die analytische Beschreibung zeigt die Auswirkungen des Leistungsbedarfs am Ausgang auf die Eingangsimpedanz des Ladungspumpen-Gleichrichters, welcher als Kernelement des Energiewandlers fungiert. Diese Eingangsimpedanz kann als Parallelschaltung eines Widerstands und eines Kondensators aufgefasst werden, wobei sich der Widerstandswert dramatisch erhöht, wenn die am Ausgang des Wandlers abgegebene Leistung sich verringert. Die Kapazität bleibt dagegen annähernd gleich. Die vorliegende Arbeit schlägt daher den Einsatz eines adaptiven Anpassungsnetzwerkes zwischen Gleichrichter und Antenne vor, um die Effizienz des Wandlers in Abhängigkeit vom Leistungsbedarf des zu versorgenden Gerätes in verschiedenen Arbeitszuständen zu optimieren.

In passiven RFID-Transpondern ist keine Batterie eingebaut, sondern ein kleiner Speicherkondensator mit einer Kapazität im Pikofarad-Bereich, der innerhalb von einigen Mikrosekunden aufgeladen werden und als Energiespeicher (Stützkondensator) dienen kann. Bei der Kommunikation zwischen RFID-Lesegerät und Transponder sendet das Lesegerät kontinuierlich ein hochfrequentes Trägersignal aus, welches der Energieversorgung des Transponders dient. Der Leistungsverbrauch eines RFID-Transponders hängt stark von dem jeweils ablaufenden Vorgang ab. Um das Anpassungsnetzwerk elektrisch auf optimale Leistungsbertragung abzustimmen, wird eine gesonderte Stromversorgung benötigt. Das stellt bei batterielosen Geräten eine zusätzliche Herausforderung dar. Dieses Problem wird in der vorliegenden Arbeit so gelöst, dass ein Hilfsgleichrichter mit einer kleineren, konstanten Belastung eingesetzt wird, um die Regelung des Anpassungsnetzwerkes zu versorgen.

Die vorgenannte Methode wird auch angewendet während der Aufladephase drahtloser Geräte, welche Superkondensatoren als Energiespeicher nutzen. Die Aufladephase verlängert sich in diesem Fall aufgrund der groen Kapazität auf mehrere Stunden, und die Ladegeschwindigkeit wird zu einem kritischen Thema. Während des Aufladevorgangs nähert sich die Ausgangsspannung des Gleichrichters asymptotisch an, während der Ladestrom exponentiell abklingt. Die für den Gleichgewichtszustand hergeleitete Eingangsimpedanz stimmt in diesem Fall nicht ganz mit der tatsächlichen uberein, gibt aber immer noch einen sinnvollen Richtwert vor. Eine neuartige Anwendung eines adaptiven Anpassnetzwerks während transienter Ladevorgängen wurde implementiert, um das Laden der Energiespeicher drahtloser Geräte zu beschleunigen.

Table of Contents

List of Abbreviations

ADC	Analog Digital Conversion
ASIC	Application-Specific Integrated Circuit
ASK	Amplitude Shift Keying
BAN	Body Area Network
BSIM	Berkeley Short-channel IGFET Model
CCM	Continuous Conduction Mode
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Conversion
DSP	Digital Signal Processing
EHS	Energy Harvesting System
EPC	Electronic Product Code
ESR	Equivalent Series Resistor
FM0	Bi-Phase Space
FPGA	Field-Programmable Gate Array
FSM	Finite-State Machine
HEH	Hybrid Energy Harvesting
HaLOEWEn	Hardware accelerated Low Energy Wireless Embedded Sensor-Actuator Node
HF	High Frequency
IC	Integrated Circuit
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
NMOS	N-Type MOS
PCB	Printed Circuit Board
PCE	Power Conversion Efficiency
PIE	Pulse Interval Encoding
PMOS	P-Type MOS

PV	Photovoltaic
PWM	Pulse Width Modulation
RFID	Radio Frequency Identification
SDR	Software Defined Radio
SEPIC	Single-Ended Primary-Inductance Converter
SHM	Structural Health Monitoring
SOC	System on Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
TEG	Thermoelectric Generator
TPMS	Tire Pressure Monitoring System
UHF	Ultra High Frequency
UID	User ID
VHDL	Very-High-Speed Integrated Circuit Hardware Description Language
WSN	Wireless Sensor Network

List of Tables

List of Figures

Chapter 1

Introduction and Overview

Contents

1.1 Motivation

Wireless sensor network (WSN) and Radio Frequency Identification (RFID) are two emerging wireless techniques which have drawn many research interests over last decades. Wireless sensor network has been used in diverse fields, with employing a number of sensor nodes for environmental sensing (temperature, pressure, humidity, etc.) and monitoring (structural, health, etc.). RFID is mainly used for identification and tracking, like purchasing and distribution logistics, people and animal identification, international container transportation, etc.. Integrating the RFID reader with the wireless sensor node enables to combine the advantages of each [112]. By attaching on a sensor, the RFID reader can enlarge its operation area with working in a multi-hop topology [25, 130]. Battery is a traditional option to supply power for remote devices, such as wireless sensor nodes. Depending on the application, battery can support the remote devices for a certain lifetime. Recharging or changing the battery is a repeated maintenance work which is quite human-resource consuming, for those devices which are located in the places hard to reach, is even impossible. Therefore, energy autonomous sensor node has been proposed. With the aid of the auxiliary energy transducers, the remote device is able to harvest the power from the ambient/dedicated energy source, such as solar, heat and RF waves, to self-support the communication with other nodes for a lifetime unlimited by the battery capacity.

Energy sources have been explored since years, and energy transducers have been designed for various sources. Hybrid energy harvesting system, which aims to utilize different energy sources in one remote device, is proposed to supplement the single ambient energy source of which the strength is limited by the environmental situation, e.g. no sunshine available during night. Energy source like dedicated RF radiation is a promising option when ambient energy sources are insufficient.

The goal of this work is to improve the RF energy harvesting efficiency in case the load of the energy transducer is not steady, e.g. in passive transponders, the current consumption strongly depends on the task; to charge a supercapacitor, the load current of the energy transducer which flows into the supercapacitor reduces dramatically as the charges accumulate and the load voltage rises. For this purpose, the design of the RF energy transducer of variant loads is investigated, with a focus on the impact of the variant loads on the impedance match between antenna and the RF/DC rectifier.

1.2 Research Objectives

The general objective of the present thesis is to improve the RF power utilization of wireless sensor nodes and RFID readers. Many efforts have been done in power management, like to reduce the power consumption of the digital core by regularly setting it in low-power consumption mode. In this work, the focused problem is to reduce the RF power radiation which consumes the most part of the battery power, in case the remote device is used as a power source for a passive device, like RFID transponder. System-level analysis has been done and shows that by adjusting the power radiation according to the need (current consumption) of the passive devices, large amount of power can be saved.

New problems arise that, in the passive device which usually employ a RF rectifier as an energy transducer, the load current consumption is not constant but dependent on the working status of the device. Taking passive RFID transponder as an example, the current it consumes during the operation varies according to the command it executes. When harvesting RF power to charge a supercapacitor in a wireless sensor node, the current flowing into the capacitor is not constant but reduces dramatically during the charging phase. The load variation of the RF/DC rectifier greatly affects its input impedance. The traditional design is to employ an impedance matching network between the antenna and the rectifier for reducing the return loss. For a rectifier with variant input impedance, a fixed impedance matching network can not anymore guarantee the optimal power transfer for variant load current consumption. Sub-optimal power transfer due to impedance mismatch largely reduces the power transfer efficiency. For improving the power transfer efficiency in case of variant loads, in this work, it is proposed to tune the impedance matching network adaptively according to the load situation.

1.3 Thesis Outline

The thesis is organized in four main parts:

- Part I: chapter 2 as the introduction part introduces the energy harvesting techniques for wireless sensor node application. Four basic energy sources: Solar, Heat, Vibration, RF, are covered. The energy transducer for each energy source is analysed. As an example, a hybrid energy harvesting system for the bridge monitoring system is designed with converting power from solar and heat. For improving the energy conversion performance of the energy transducers, different algorithms of maximum power point tracking (MPPT) are explored. Finally as a focus of the work, different RF energy transducers at the circuit level are analyzed.

- Part II: in chapter 3, system-level analysis is done. Different topologies of integrating the RFID reader with Wireless Sensor Networks are summarized, and analysis shows the importance of improving the power utilization of the RFID reader to prolong the battery life. Methodology has been proposed to improve the power utilization by tuning the power radiation of the RFID reader according to the need of the transponders during both power-up phase and communication phase. A digital core of RFID transponder is designed, and the power consumption variation in the time domain is investigated, and the results imply a possibility of reduce the energy consumption of the reader with adaptively changing the power radiation of the reader. In the transponder side, a supporting design modification shall be implemented. Due to the change of the current consumption of the transponder, the input impedance of the rectifier changes, which requires to adjust the matching network between the rectifier and the antenna to maintain the optimal power transfer.

- Part III: chapter 4 focuses on the RF/DC power converter design. The dependency of the input impedance of the rectifier on the load current consumption is investigated. Analytical derivation has been done to express the input impedance as a function of the load current. To maintain the optimal power transfer from the antenna to the rectifier, the matching network which located in between is suggested to be tuned according to the change of the load current consumption. For demonstration, a rectifier is designed with employing an auxiliary rectifier for generating feedback control signals to tune the matching network.

- Part IV: in chapter 5, the input impedance variation of the rectifier during the charging-up process is investigated. It has been found that, by adjusting the matching network according to the change of the input impedance during charging-up phase, the charging speed can be significantly improved, and in the power radiator side, a large amount of power can be saved. A PCB design has demonstrated the propose. Finally, in chapter 6, a summarization of the work is given, and a directive outlook has been suggested.

Chapter 2

Energy Autonomous Wireless Sensor Nodes

Contents

2.1 Wireless Sensor Networks

2.1.1 Application Profile

Wireless sensor networks (WSNs) consist of a number of sensor nodes, which are able to collect information from the environment by measuring diverse environment variables, like temperature, humidity, sound etc.. The wireless sensor networks have been employed in many applications of different areas, like Structural Health Monitoring (SHM) [44, 68–70, 83], energy efficient/smart buildings, medical diagnostic/health monitoring with personal body area network (BAN) [19, 75, 84], automotives [36, 109], precision agriculture etc.. Wireless sensor network is also a potential candidate for many emerging technologies: smart grids, etc.. Some representative applications are briefly presented in this section.

- Structural Health Monitoring: Monitoring civil infrastructure in real time becomes essential for predicting and identifying the structural damage caused by excessive use or natural catastrophes. The sensor nodes are localised in the structures for information acquisition (e.g. vibration characteristics of a bridge) [82]. A sensor network is employed in the structures that the data obtained by scattered sensor nodes is processed/compressed and sent to the base station via wireless communication.

- Energy Efficient Smart Buildings: Improving energy efficiency in the buildings is a rising concern. As estimated by the European Commission [29], 40% of EU's total final energy consumption and CO_2 emissions are due to the energy use in residential and commercial buildings. Wireless sensor networks have been applied to sense the presence of human beings, as well as the light and temperature of the buildings for automatically controlling the lightning and heating/air conditioning system [101, 105, 125].

- Automotives: Wireless sensor networks have drawn much interest in automotive industries for safety and control applications, of which, tire pressure monitoring system (TPMS) is a representative example. By mounting a sensor in the tire, pressure and temperature of the tire can be measured for controlling the tire wear. Further functionalities, like measuring the load situation and the friction of the tire, can be used to enhance other safety systems [120]. Energy-autonomous TPMS has been developed to miniaturize the device for flexible installation and reduce the battery-maintenance cost [107]. New applications of WSNs in automotives, like condition monitoring, prediction and acknowledgment of the abrasion loss or function failure of the vehicle components, are under investigation [109].

- Precision Agriculture: The application of applying wireless sensor networks in precision agriculture has been promoted over years. Through monitoring the changes of the environment in real time, it is possible to enable a precise and fast response, such as irrigation, with meanwhile saving abundant human labor. With employing sensors in the farm to sense the soil moisture, large amount of water can be saved during the irrigating. In such application scenario, energy-autonomous sensors are desired for long-term use and less maintenance cost.
- Smart Grids: Traditional electric power grid suffers from the increasing energy burden and lack of monitoring and fault diagnostics, which have been the main causes of several major blackouts. New concept of a smart grid with secure and reliable infrastructure has been defined. The smart grid is able of improving the power delivery efficiency, reliability and safety, as well as smoothly integrating/deploying renewable and alternative energy sources with intelligent monitoring and communication technologies. Flexible and cost-effective wireless sensor networks have prospective application in the smart grid, to replace the traditional wired monitoring systems and enable the residential energy management [27,41].

2.1.2 Architecture and Design Space Exploration

A sensor node is a tiny, intelligent device, which is composed of four parts [2]: sensing unit, processing unit, transceiver unit and a power unit, as shown in Fig.2.1. Each node can be equipped with one or more sensors, which are flexibly installed in variant locations for long-term environment sensing: temperature, speed, light, pressure etc.. The

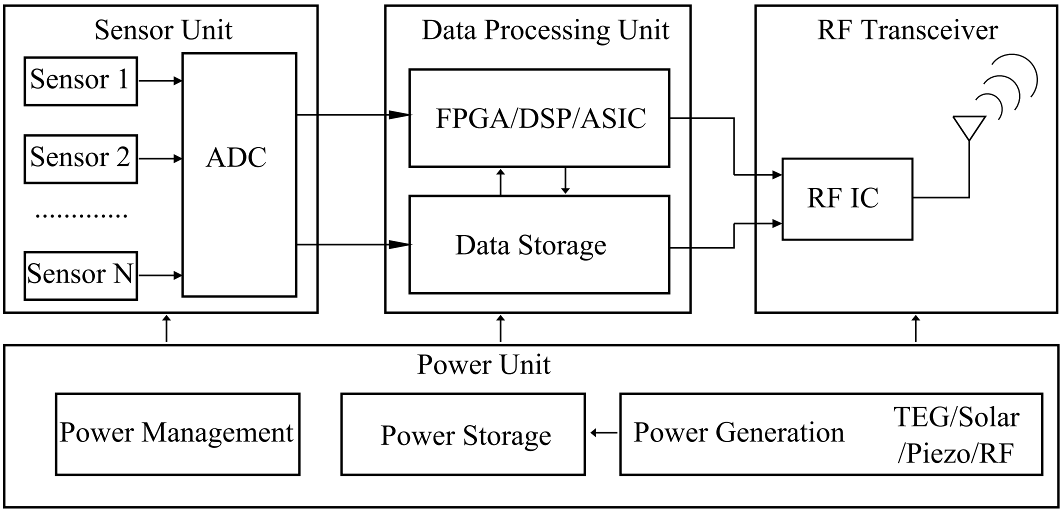


Fig. 2.1: Design Architecture of a Sensor Node

data obtained from the environment is sampled by a A/D converter and then sent to the processing unit for further computation or storage. Depending on the application specifications, different data processors (FPGA, DSP, ASIC) can be chosen. The useful information is then sent to the base station with a RF transceiver. Besides the data transmission, there is a power unit, which usually contains a power storage unit (battery or super-capacitor) and a power management circuitry to improve the energy utilization of the node. Among those parts, the transceiver unit consumes the most power during communication with other nodes or base station.

To power up a sensor node, an electricity storage device like battery can be used, and depending on the battery volume as well as the amount of the power consumption of the sensor node, a certain lifetime (around a year) of the sensor node can be achieved. With a limited battery capability, the sensor node can communicate with very restricted distance. In applications where the sensor nodes are scattered in a smaller-scale physical range, the sensor nodes can communicate with base stations with sending the samples to or receiving command from the base station with consuming a small amount of power. However, in applications where the sensor nodes are located in a large open field, the sensor nodes are not capable of communicating with the base station. The sensor shall send the data by hopping through other nodes following the defined network topology, like tree, star or mesh, which reduces the power consumption of the transceiver unit and improves the data transmission reliability.

Most commercial wireless sensor nodes are still battery based. Depending on the application, the sensor nodes are installed in various locations. Repeated maintenance of the battery (change or recharge the batteries) is quite a human resource consuming work, and for those locations hard to reach, even impossible. To extend the lifetime and to improve the energy autonomy of the wireless sensor nodes, energy harvesting techniques are investigated to online recharge the energy storage device-battery or super-capacitors. Potential energy sources from the ambient environment are: sunshine, heat, vibration, wind, RF waves etc.. The energy sources have different power level, and for each, the energy transducer (solar panel, Seebeck thermal electrical generator, piezoelectric, charge pump) provides various ability of converting harvested power to electricity. Tab.2.1 summarizes the characteristics of different energy sources and the typical conversion efficiency of energy transducers. For each energy source, specific energy transducer is required, and thus particular power management circuit design.

In the following sections, energy harvester designs for different energy sources: Solar, Thermoelectric, Piezoelectric and RF wave are introduced, and finally a design example of hybrid energy harvesting system (HEH) with the target application of bridge health monitoring is described.

Tab. 2.1: Comparison of Energy Sources and Transducer Efficiency

Energy Source	Source Power	Energy Transducer Efficiency / Induced Power Level	Reference
Solar light	Outdoors $0.1W/cm^2$ Indoors $0.1mW/cm^2$	3.5%-32%	[40]
Vibration	Human $1m/s^2$ @ 50Hz Industrial $10m/s^2$ @ 1KHz	$4\mu W/cm^2$ $100\mu W/cm^2$	[120]
Thermal Energy	Human $20mW/cm^2$ Industrial $100mW/cm^2$	$0.8\% - 2.7\%$	[120]
RF wave	Ambient Source (GSM Base Station) $0.01\mu W/cm^2$(100m) - $0.3\mu W/cm^2$(25m) Dedicated Source (EIRP 4W) $1.27\mu W/cm^2$ (5m)	$\sim 30\%$	[118]

2.2 Solar Energy Harvester

Small solar panels have been widely employed in wireless sensor nodes to improve the energy autonomy of the system by converting the incoming photons into electricity. In the direct sunshine outdoors, the solar irradiance can achieve $0.1W/cm^2$ at the earth surface. The power conversion efficiency of a solar cell can range from 3.5% to 32% depending on the design material measured under the global AM1.5 ($1000W/m^2$) at $25°$C [40]. The typical usage environment of the solar energy harvester is outdoor installations [1], e.g. bridge health monitoring, road sensing, precision farming and irrigation control, etc..

2.2.1 Characterization of Photovoltaic Cell

The output characteristics of the photovoltaic cell nonlinearly depend on the environment conditions: temperature or irradiation density. The output impedance is not a constant one, but strongly depends on the environment condition. Fig.2.2 shows the equivalent circuit of the photovoltaic (PV) module. The characteristic equation of the PV module [48] [60] is given by Eqn.2.1:

$$I_L = I_{LG} - I_{sat}\{e^{\frac{q}{AKT}(V_L+I_LR_S)} - 1\} - \frac{V_L + I_LR_S}{R_{SH}} \tag{2.1}$$

where I_L and V_L are the output load current and voltage; I_{LG} is the light-generated current which depends on the cell temperature and the light irradiation; I_{sat} is the reverse saturation current of the diode and is dependent on temperature and design material; q

is the electronic charge, A is diode ideality factor; K is the Boltzmann's constant; T is the temperature in Kelvin; R_S is the series resistance; R_{SH} is the shunt resistance.
The output characteristic of the solar cell is plotted in Fig.2.3, where V_{MPP} and I_{MPP} are the output voltage and current of the solar cell when the maximum power is transferred to the load, and P_{MPP} is the maximum output power. The data is based on the parameters extracted for blue solar cells [49], refer to Tab.2.2. Fig.2.4 shows the drift of V_{MPP} when the irradiance condition changes. Further, the equivalent load impedance is neither a constant one, e.g. during the charging process of a supercapacitor, the equivalent impedance increases dramatically with the voltage raising and current reducing. To ensure the energy harvesting system continuously work with the maximum power transfer efficiency, maximum power point tracking techniques were proposed to match the load to the energy source.

Tab. 2.2: Parameters for I/V characteristic of Solar Cell

Parameter	R_S	R_{SH}	I_{sat}	I_{LG}	A
Unit	$m\Omega$	Ω	μA	A	-
Value	68.26	1000	0.1036	0.1023	1.5056

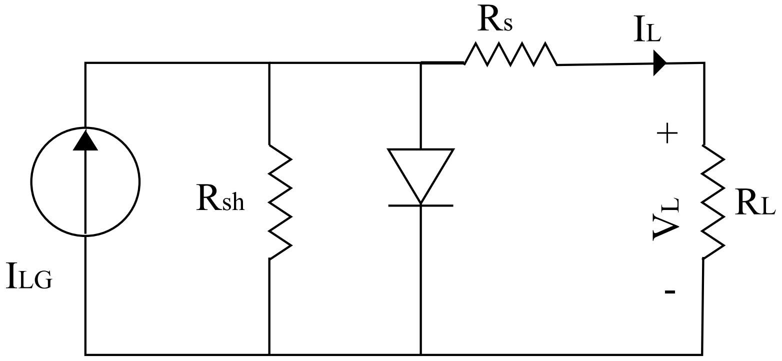


Fig. 2.2: Equivalent Circuit of a Photovoltaic Module

A switch-mode DC/DC converter is usually used to convert the output voltage of the solar cell to a certain voltage for charging the battery/supercapacitor. Fig.2.5 shows a SEPIC (Single-Ended Primary-Inductance Converter) DC/DC converter [31], which has the ability of regulating an input voltage larger or smaller than the output voltage. By tuning the duty cycle of the PWM signal, the input impedance of the DC/DC converter can be adjusted such that impedance match is achieved at the solar cell output interface. Assuming the converter operates in the continuous conduction mode (CCM), the duty cycle of the SEPIC converter shall be set as:

$$D = \frac{V_{OUT} + V_D}{V_L + V_{OUT} + V_D} \tag{2.2}$$

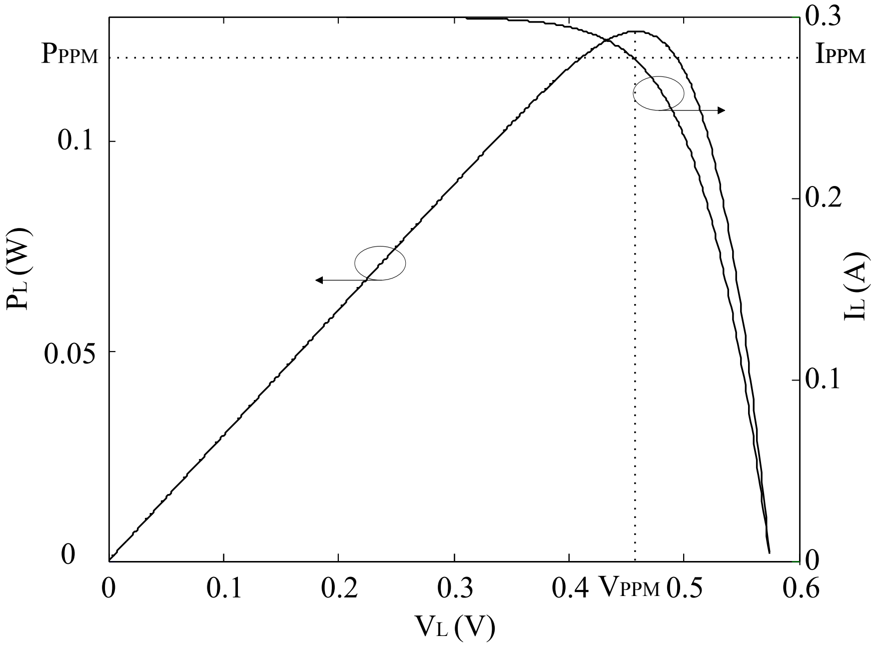


Fig. 2.3: I/V, P/V plots of the Solar Cell

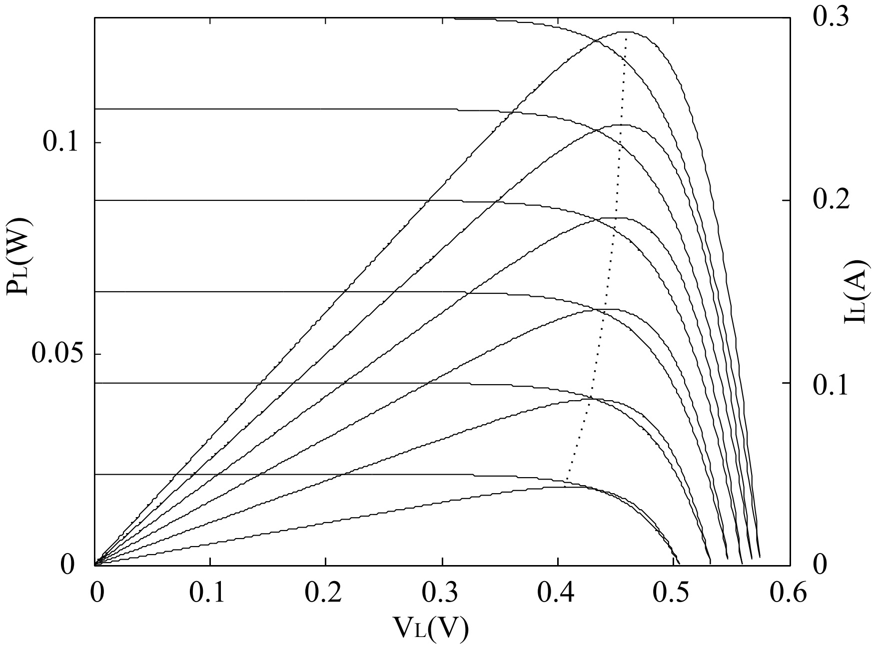


Fig. 2.4: Drift of the Maximum Output Power Point According to the Irradiance Conditions

where, V_{OUT} is the regulated output voltage of SEPIC converter; V_L is the output voltage of the solar cell; V_D is the forward voltage of the diode. With a fixed regulated output voltage for charging the battery and a certain forward voltage of the diode, the duty cycle is determined by V_L. For different irradiance situations, the optimal voltage output of the solar cell V_{MPP} drifts, for which duty cycles should be tuned to track the maximum power output point.

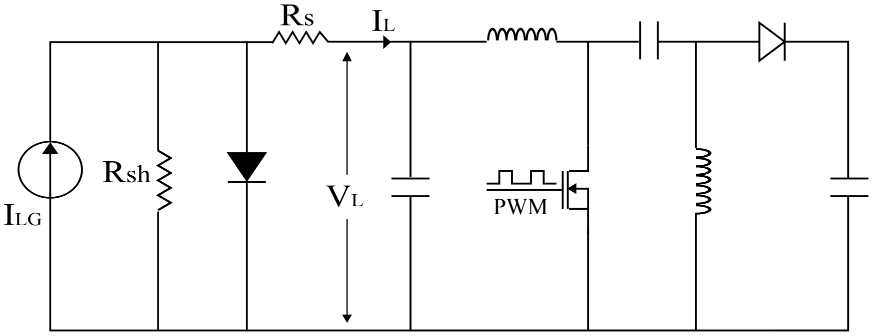


Fig. 2.5: Switch Mode DC/DC converter

2.2.2 Maximum Power Point Tracking Techniques

Different MPPT techniques have been exploited: hill-climbing, perturb and observe, incremental conductance, fractional open-circuit voltage, fractional short-circuit current, etc.. Esram et al. [28] has summarized various MPPT techniques and compared them in different aspects: the implementation complexity, sensors used for MPPT algorithms, costs etc.. Different techniques will be revised, and some of them were employed in the following design examples. The following described techniques are all based on a common design with connecting the PV arrays with a DC/DC converter, and the maximum output power point is reached by tuning the duty cycle of the voltage converter.

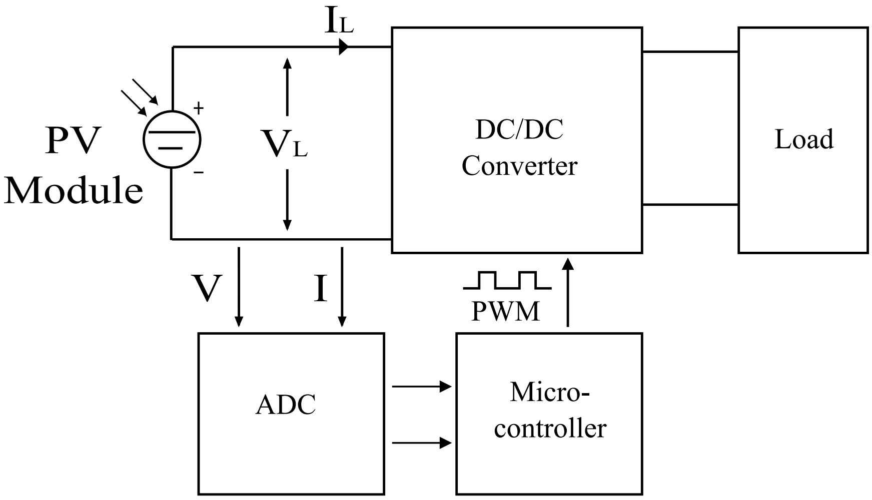


Fig. 2.6: Block Diagram of Microcontroller-Based MPPT system

2.2.2.1 Periodical Searching

A direct way of finding the maximum output power point is to record the output power P_L of the PV array with sensing the output voltage and current by tuning the duty cycle D of the voltage converter over the whole period (from 0 to 1) with a certain step. The maximum value is searched among the recorded data, with which the optimal duty cycle can be found. The process is run periodically to follow the environment change. To implement such a technique, A/D converters are needed to sample the output voltage and current of the PV array, and a microcontroller is needed to record the data and finding the maximum value for the output power, according to which further tune the duty cycle of the PWM signal. The block diagram of the harvesting platform with this technique is shown in Fig.2.6. This technique uses a very simple algorithm to track the maximum power point. However, the power consumption of the microcontroller is high due to the continuously searching and comparing.

2.2.2.2 Hill Climbing / Perturb and Observe

In case of connecting the solar cell to a DC/DC converter, Hill Climbing technique [60, 115, 124] tunes the duty cycle of the converter with a small step. For each step, with the aid of a A/D converter and a microcontroller, as shown in Fig.2.6, the output current and voltage of the solar cell are sampled and the output power is then calculated. The output power is then compared with that obtained in the previous step, and the tuning direction of the duty cycle is determined. The process continues until the maximum power point is reached.

Perturb and Observe (P&O [34, 50]) shares a same principle as Hill Climbing. Instead of perturbing the duty cycle, P&O perturbs the output voltage of the photovoltaic module to search for the maximum power point. Compared with Periodical Searching, Hill Climbing and P&O trace in a smaller extent of the duty cycle / PV voltage, and the searching work load is reduced. The main drawback of the two methods is the operation point oscillates around MPP when the perturbation step size is big [15, 28]. To minimize the oscillation, the perturbation step size shall be reduced, with tradeoffs of increased searching duration and power consumption of the processing unit.

2.2.2.3 Increment Conductance

Increment Conductance (IncCond) [55,61,128] is a derivative algorithm of the Hill Climbing and P&O, which are based on the power characteristic of the PV array, as shown in Fig.2.3. The derivative of the power output over voltage output dP/dV indicates the current operation point referring to the optimal operation point: when dP/dV is larger than 0, the current operation point is on the left side of the optimal operation point; when it is smaller than 0, the current operation point locates on the right side of the optimal operation point; once it equals to 0, the current operation point is the optimal operation point. Since the dP/dV can be approximately written as $I + V\frac{\Delta I}{\Delta V}$, the algorithm can instead observe the incremental conductance ($\Delta I/\Delta V$) of the photovoltaic module, and the optimal operation point is achieved when the incremental conductance equals to $\frac{-I}{V}$.

IncCond cannot fundamentally solve the oscillation problem which are encountered in the Hill Climbing/P&O methods [34], and encounter the expense of slower tracking speed by improving the accuracy with reducing the increment size of the conductance.

2.2.2.4 Fractional Open-Circuit Voltage

Fig.2.7 shows the approximately linear relationship between the open voltage V_{OC} and the optimal output voltage V_{MPP} under varying environment situations: varying irradiance and temperature.

$$K_{FOC} = V_{MPP}/V_{OC} \tag{2.3}$$

Based on it, the fractional open-circuit voltage method has been developed with measuring the open voltage by periodically disconnecting the solar panel from the DC/DC converter, or employing a pilot solar cell [42]. This method only approximately indicates the optimal operation point, but the implementation of the method is much simpler comparing with the former methods.

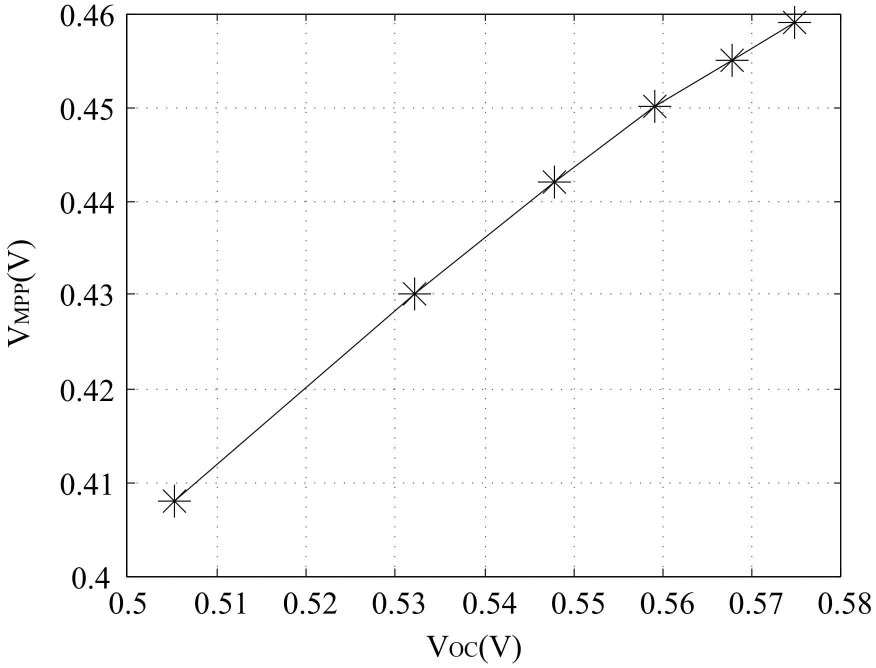


Fig. 2.7: Nearly Linear Proportional Relationship between V_{OC} and V_{MPP} under Different Irradiance Conditions

2.2.2.5 Fractional Short-Circuit Current

Fractional Short-Circuit Current [74] is based on the fact that the short circuit current of the PV module has a nearly linear relationship with the optimal current. By shorting the PV module with an extra switch, the short circuit current can be measured periodically with a current sensor. Once the fractional factor is determined, the algorithm can be implemented with building a lookup table in the control unit. Comparing Fractional Short-Circuit Current with Fractional Open-Circuit Voltage, both are based on a linear approximation and achieve no exact optimal power output. Besides, Fractional Short-Circuit Current requires more devices for sensing the current.

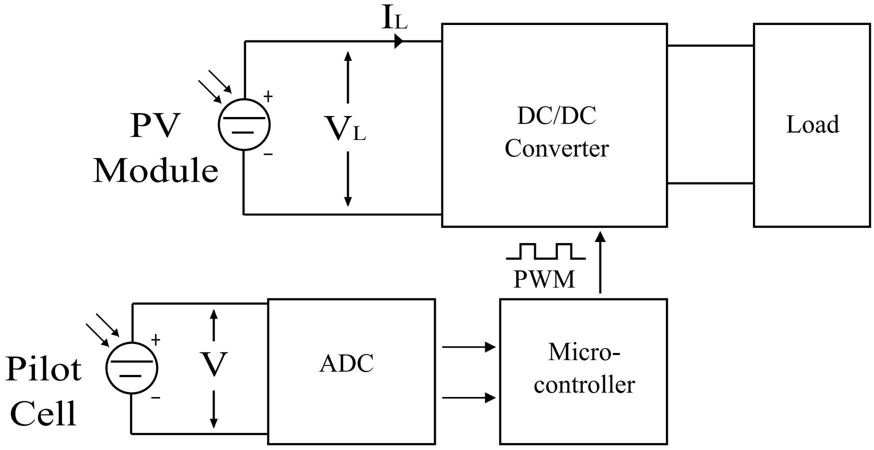


Fig. 2.8: Block Diagram of Harvester Platform with Pilot Cell

2.2.3 Solar Energy Harvesting Circuit Design

2.2.3.1 Performance of Employed Solar Panel

Tab.2.3 listed the technical data of the employed solar panel in the following design example. For a commercial solar panel of a size $12.5cmX6.5cm$, the open circuit voltage can vary between 0V and 9.5V. Fig.2.9 shows the recorded voltage output of the employed solar panel from 12.August 2011 to 18.August 2011. The solar panel is attached to the window which faces the south direction. Fig.2.10 depicts the output power changing with the load impedance when the solar irradiance varies, from which it can be seen that the load has a strong effect on the induced output power, and for different irradiance situations, it is desirable to match the solar panel with different loads for maximum induced power.

Tab. 2.3: Technical Data of Employed Solar Panel

Parameter	Unit	Value
Dimension	cm^2	81.25
Open Circuit Voltage V_{OC}	V	9.33
Optimal Voltage V_{MPP}	V	7.29
Optimal Current I_{MPP}	mA	11.3

2.2.3.2 Power Management Circuitry Design

In this design example, fractional open circuit voltage method is implemented. The PV array is periodically disconnected from the voltage converter with setting the duty cycle to 0. The PV array is tested offline under various irradiance to obtain the proportion fac-

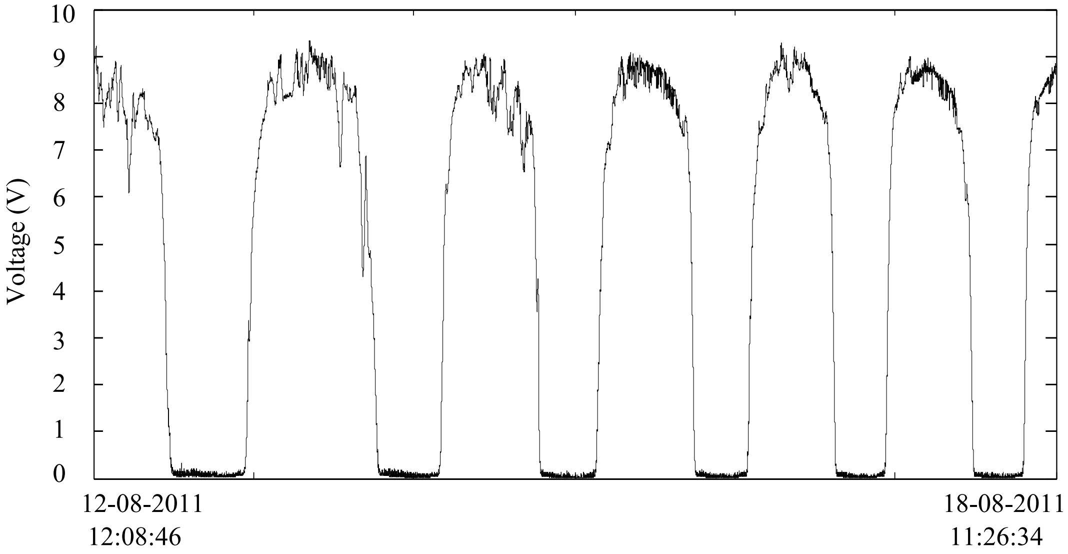


Fig. 2.9: Measured Open Voltage Output of the Employed Solar Panel

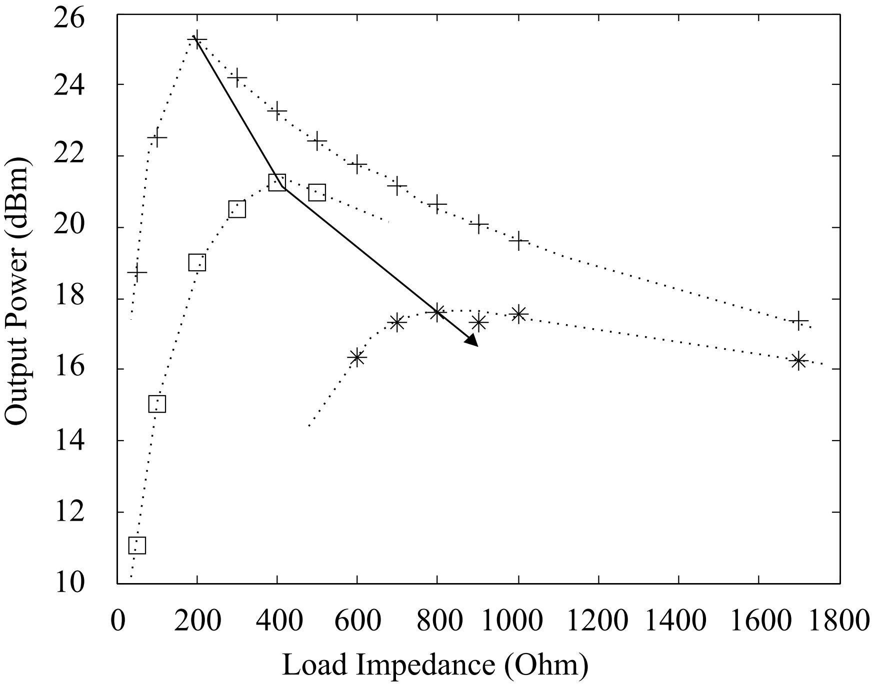


Fig. 2.10: Measured Output Power of the Employed Solar Panel v.s. the Load Impedance

tor K_{FOC}. The measured open circuit voltage together with the optimal voltage is listed in Tab.2.4, and the fractional factor ranges in a small scale from 0.73 to 0.78.

Fig.2.11 shows the maximum power point drifts with the tuning of the duty cycle of the PWM signal applied to the DC/DC converter. For further design, the duty cycle for optimal voltage output depending on the open circuit voltage is tested, as shown in Fig.2.12. The duty cycle can be adjusted to track the maximum power point with the aid of a lookup table built based on the measurement of the open circuit output voltage.

The designed solar energy harvesting circuit is shown in Fig.2.13. A low power FPGA

Tab. 2.4: Fractional Factor K_{FOC}

Open Voltage V_{OC} (V)	7.434	7.763	8.224	8.581	8.92	9.184	9.333
Optimal Voltage V_{mpp} (V)	5.421	5.68	6.117	6.64	6.6	6.91	7.29
K_{FOC}	0.729	0.7318	0.7438	0.774	0.74	0.752	0.781

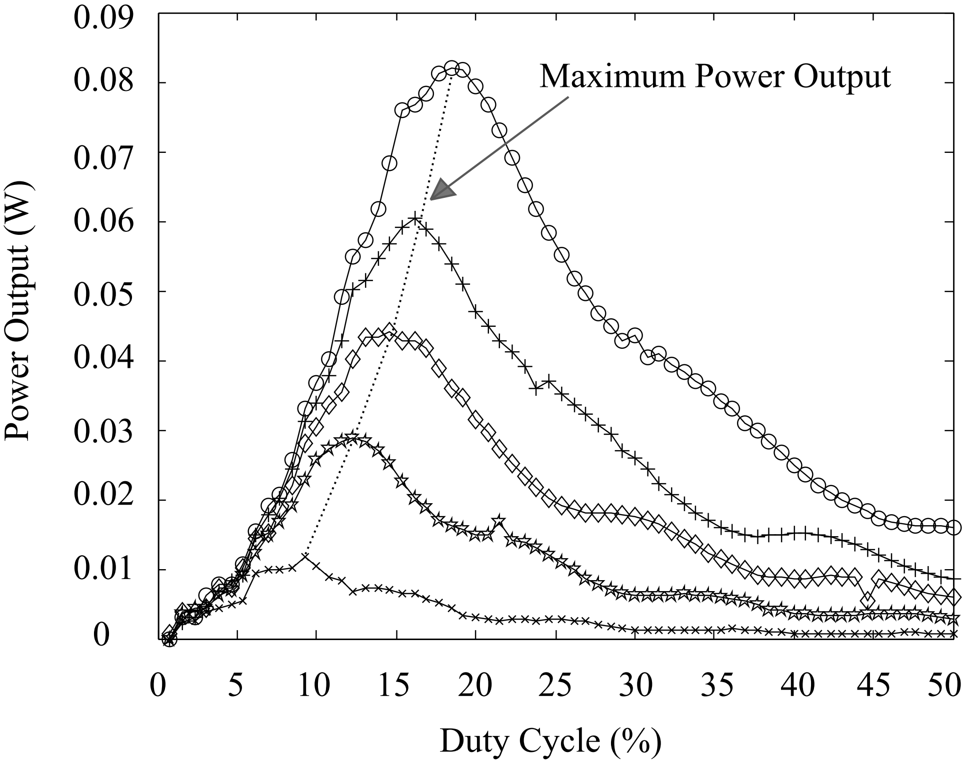


Fig. 2.11: Measured Output Power v.s. the Duty Cycle of the PWM Signal

is employed, and the lookup table is stored in the FPGA. For powering the FPGA, two voltage regulators are used for obtaining 1.5V and 3.3V, respectively. An A/D converter is used to sample the open circuit voltage of the PV module V_{OC} when the duty cycle is set as 0 by the FPGA, and the sampled data is then sent to FPGA for finding the optimal duty cycle D_{MPP}. Due to the environment situation (nights, cloudy weather), the power drawn from the battery for powering the auxiliary circuits: voltage regulators, ADC and FPGA, may be larger than the power harvested from the PV module. When such case happens, the auxiliary circuits shall be switched off to save power. A hysteretic comparator is used to compare the fraction of the current V_{MPP} with a reference voltage. Base on the comparison, when the fraction of V_{MPP} is smaller than the reference voltage, a shut down signal is generated by the comparator and sent to the voltage regulations, with which, the auxiliary circuits are shut down. Once the power harvested from the PV module arises, the voltage regulators are started again as well the auxiliary circuits.

For demonstration, the power harvested by the solar cell is used to charge the Li-ion battery of a capacity of 4.6AH. Two charging procedures with and without MPPT algo-

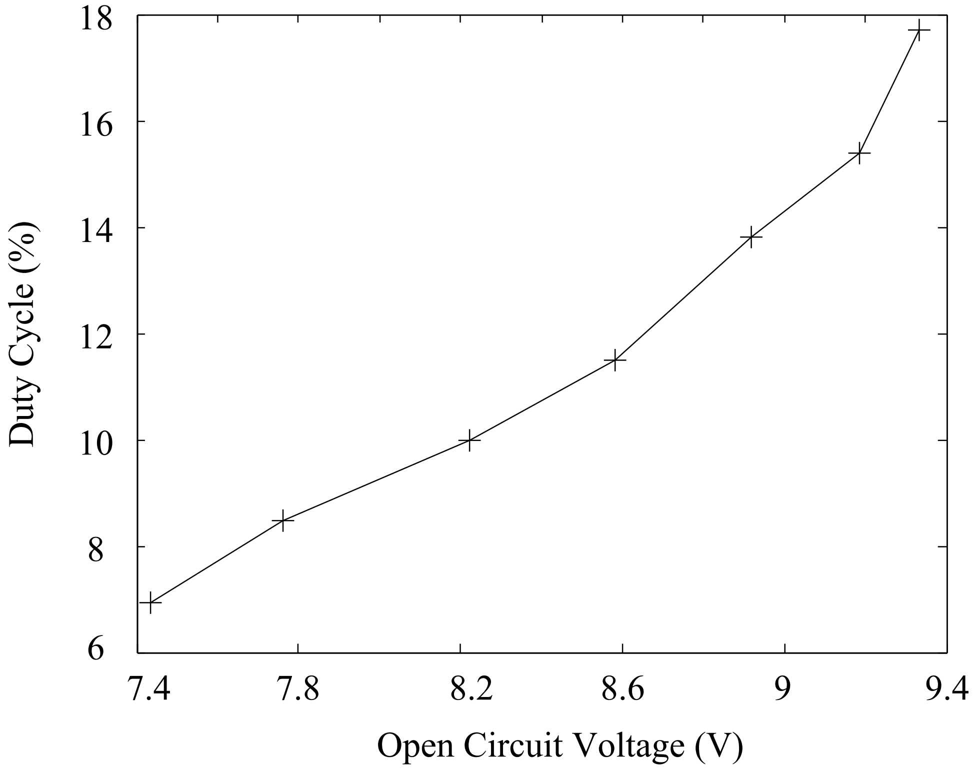


Fig. 2.12: Measured Optimal Duty Cycle v.s. the Open Circuit Voltage

rithm are recorded simultaneously, as shown in Fig.2.14. The charging procedure has been started on 01.09.2011 and stopped on 13.09.2011. The strength of the radiated light is recorded with measuring the induced voltage of an open-loaded solar cell. The blue line indicates the charging procedure with the maximum power point tracking algorithm - Fractional Open Circuit Voltage, while the charging procedure with a fixed duty cycle is represented by the green line. The results show that the battery is charged much faster with employing the MPPT algorithm. The designed platform can be used for comparing different algorithms with considering the power consumption caused by implementing the algorithm.

2.3 Thermal Energy Harvester

In industry, many types of thermodynamic heat engines have been developed to convert the thermal power to other types of power, such as mechanical work, electricity etc.. A typical application of the heat engine is the internal combustion engine in automobiles, where the combustion of the fuel produces heat and gases with high temperature and high pressure, which further generates the mechanical energy by applying a direct force to the pistons. In wireless sensor network, to improve the energy-autonomy, it is desirable to harvest the power from the ambient heat sources. The traditional heat engine mechanism is not applicable due to its high design complexity and the need of a large

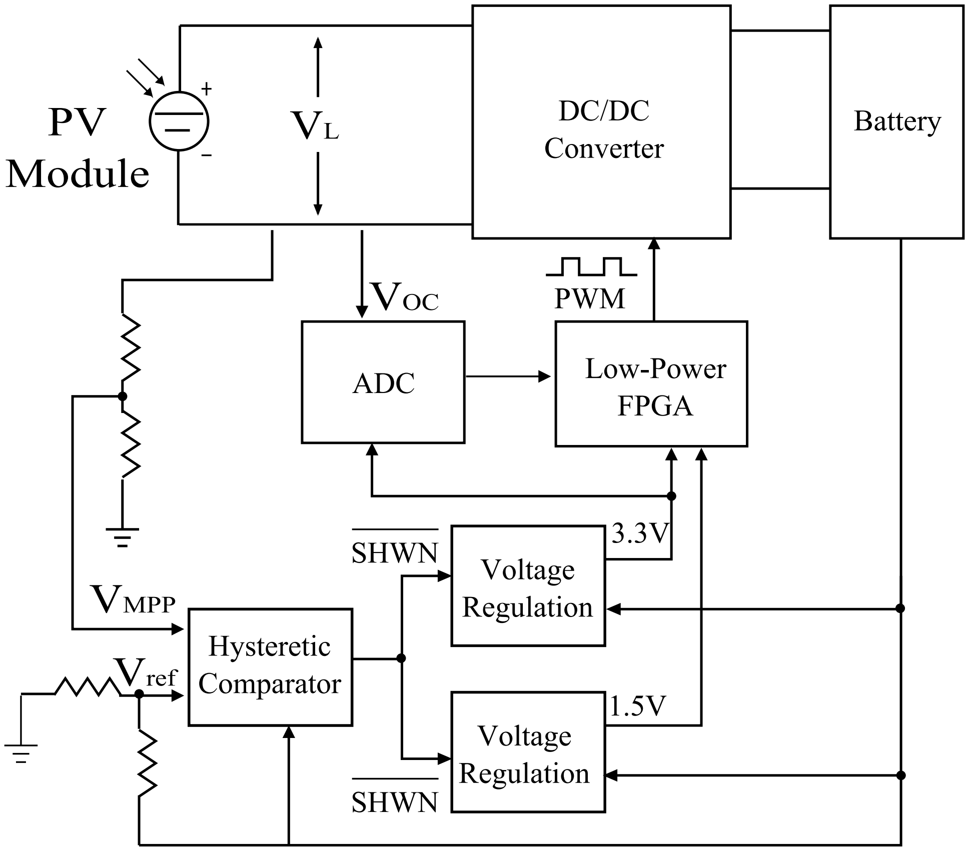


Fig. 2.13: Block Diagram of the Designed Solar Energy Harvesting Circuit

amount of dedicated energy sources like fuel.

To harvest power from ambient heat source, energy transducer, which is capable to convert low temperature difference to electricity, is needed. The most common thermal energy transducer applied in wireless sensor network is the thermoelectric generator based on Seebeck effect, which can be observed in a conductor/semiconductor. When different temperatures are applied at two different points of the conductor/semiconductor, a voltage difference will be generated. A thermocouple, which is widely used in thermoelectric energy generators and temperature sensors, is based on Seebeck effect, where two different conductors/semiconductors are connected in serial. When the temperatures of the two junctions of each conductor/semiconductor are different, a voltage proportional to the temperature difference will be produced, please note the function diagram of the thermocouple in Fig.2.15. Seebeck coefficient S is defined to characterize the material, which is the ratio between the developed voltage difference and the applied temperature difference, i.e.:

$$S = \frac{dV}{dT} \tag{2.4}$$

The Seebeck coefficient depends on both the material of the conductor/semiconductor and the temperature. For n-doped alloys, the Seebeck coefficient is negative, and for p-doped ones, it is positive, as the charge carrier (electrons and holes) flowing from the hot side to the cold side of the material [43]. In the thermocouple, one n-type semiconductor

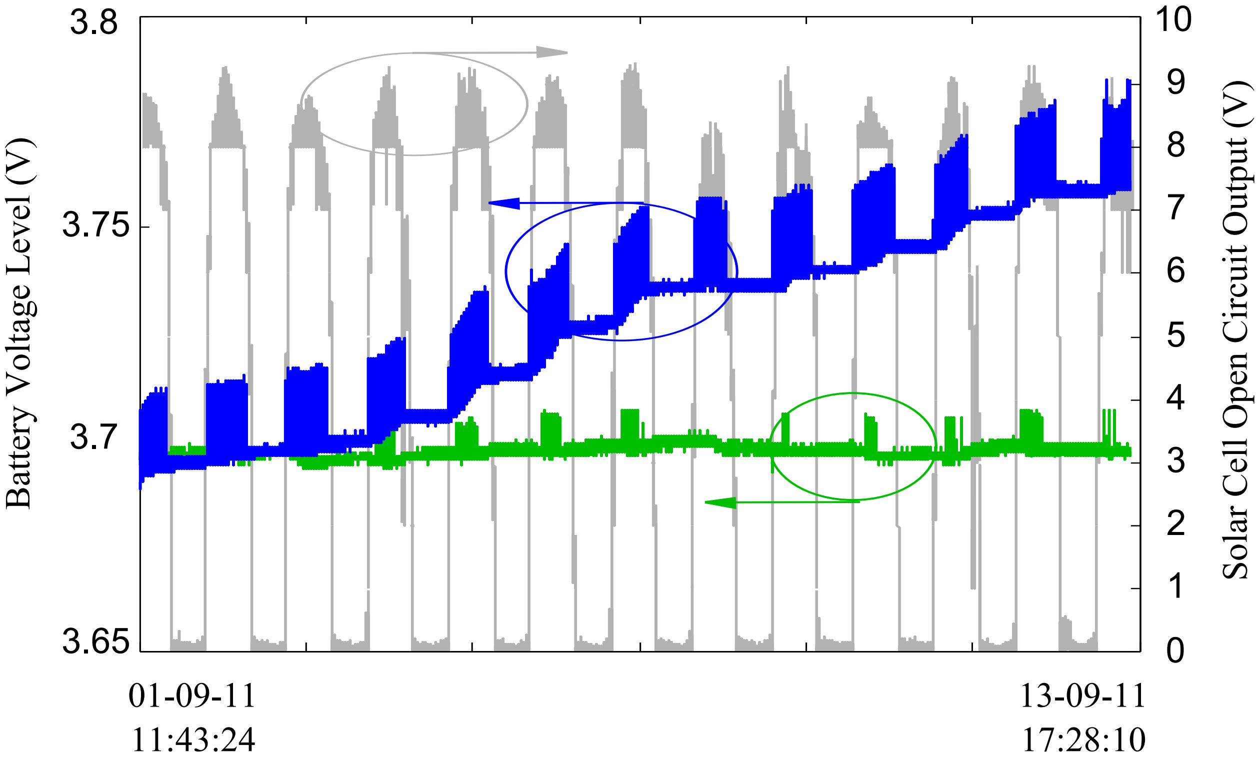


Fig. 2.14: The Battery Charging Procedure with (Blue Line) and without MPPT Algorithm (Green Line).

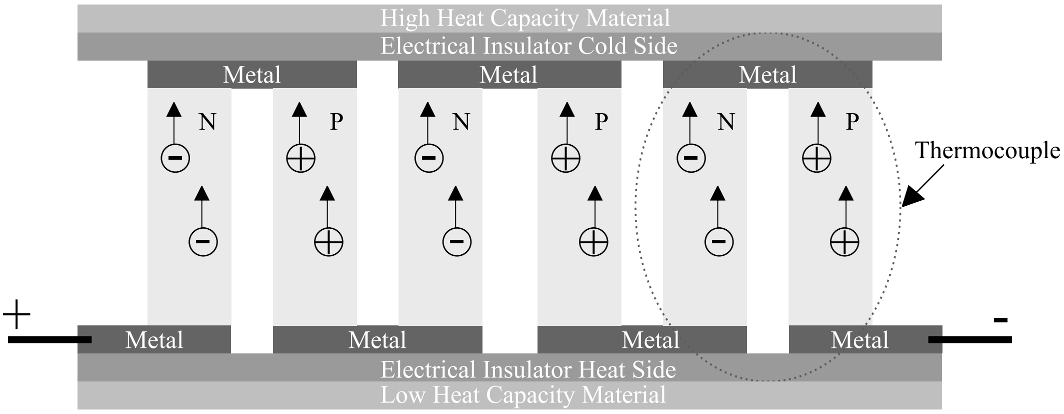


Fig. 2.15: Diagram of Thermoelectric Generator with Thermocouple Unit

and one p-type semiconductor are connected in serial. The generated voltage potential is then dependent on the difference between the Seebeck coefficients of the two different materials, i.e.:

$$V = \int_{T_C}^{T_H} (S_P - S_N) dT \tag{2.5}$$

where, T_C and T_H are the temperatures of the cold and hot sides, individually, S_P and S_N are the Seebeck coefficients of the n- and p-type semiconductors.

2.3.1 Thermoelectric Materials and Figure of Merits

Besides the Seebeck coefficient, thermal and electric conductivities are also important parameters to the efficiency of the thermoelectric generator [121]. For example, materials, with higher carrier concentration like metal or heavily doped semiconductors, have high electric conductivity, but lower Seebeck coefficient and higher thermal conductivity. Materials, which are good electrical conductors, are mostly also good thermal conductors, like metals, which can hardly maintain the temperature difference. By considering the thermal conductivity κ and electric conductivity σ, a thermoelectric figure of merit Z is defined as:

$$Z = \frac{S^2 * \sigma}{\kappa} \tag{2.6}$$

A dimensionless figure of merit ZT is defined as the product of Z and the average temperature, which is used to measure the efficiency of the thermoelectric materials [43]. Good thermoelectric materials must have high ZT, which means large Seebeck coefficients, high electrical conductivities and low thermal conductivities to maintain the heat at the junction and to reduce the heat transfer losses [23]. Semiconductors with proper carrier concentration are most widely used as thermoelectric materials due to compromise between the thermal and electrical conductivities. The most commonly used thermoelectric material has a ZT around 1 [117]. A peak ZT of 1.4 at 100^oC in a p-type nanocrystalline BiSbTe bulk alloy has been reported in [88].

2.3.2 Heat Source

There are abundant ambient heat sources in the environment: solar heat, industrial waste heat, human body etc..

- Solar: In addition to be directly converted to electricity with photovoltaic arrays, solar energy is a rich heat source. Technology has been developed to convert the solar energy to heat: solar thermal energy. The heat harnessed by the solar thermal collector can be used in many aspects, ranging from residential use, like heating water to industrial use, like electric power plants. Thermal mass materials, like water or concrete, which has high heat capacity, are used to collect and store the heat during the day and release later during the night. A thermoelectric generator can be used to convert the collected heat to electricity for powering the wireless sensor nodes, as presented in [65, 129]. Yu et al. attached the hot side of the thermoelectric generator in the backside of the solar panel, while the cold side with a heat sink to increase the temperature difference. Since the solar panel is directly exposed in the sunshine, the temperature is higher than that of the heat sink which is located in the shadow, even the thermal capacities of the two are quite close. In the structure proposed by Yu et al., the thermal energy harvester operates only during the daytime together with the solar energy harvester.

Another approach is to apply the concept of solar thermal energy technology in designing thermoelectric energy harvesting system. The thermal mass material which can be attached in one side of the thermoelectric generator stores the heat during the day. In the other side, a material with low heat capacity, like iron, of which the temperature raises rapidly when exposed in the sunshine, can be used. The hot and cold side of the thermoelectric generator exchange during the day and night. During the day, the temperature of the thermal mass material rises slowly while storing the heat due to its high heat capacity. Conversely, the temperature of the lower heat capacity material rises rapidly with the solar irradiance. During the night, the thermal mass material releases the heat and the temperature drops slowly; by contrast, the temperature of the low heat capacity material drops drastically and becomes colder than the other side. The output voltage changes the polarity as the hot and cold sides exchange. Therefore, a rectification circuit is needed at the output of the thermoelectric generator.

- Waste heat: Industrial waste heat is another free heat source. Power stations, vehicle engines and some industrial plants, like steel making, generate a huge amount of waste heat. Before employed in the wireless sensor networks, the thermoelectric generator has been widely used in recovering the waste heat [92]. The heat exchanger, which is attached on the hot and cold sides of the thermoelectric generator to retain the temperature, is crucial for the recovery efficiency [73]. When installing wireless sensor nodes in the location where waste heat is available, it is applicable, sometimes even necessary to reuse the energy by converting the waste heat to electricity. Draney et al. [22] developed ”smart bearing” sensor which can be installed in a harsh environment like tube engine, where the environment temperature is too high that the battery can not bear. To power such a sensor, the waste energy is harvested.

- Human Body: The temperature difference between the human body and the surrounding air can utilized to power a low power consumption device [56,64] which is attached to the human’s skin with the help of a thermoelectric generator. Another application of the thermoelectric generator is to supplement the battery of the implanted biomedical device by harvesting the power from the slight temperature difference between the inner surface of the body skin and the core body [122].

2.3.3 Equivalent Electrical Model and Interface Property

The heat flow into the hot side of the thermocouple Q_H and the heat flow out of the cold side is Q_C can be expressed as [18,97,98]:

$$Q_H = S_{pn} T_H I_L + K(T_H - T_C) - \frac{1}{2} I_L^2 R_{in} \tag{2.7}$$

$$Q_C = S_{pn}T_C I_L + K(T_H - T_C) + \frac{1}{2}I_L^2 R_{in} \tag{2.8}$$

where, S_{pn} is the difference of the Seebeck coefficient of the semiconductors used in the thermoelectric element; K is the thermal conductivity of the material; T_H and T_C are the temperature of the hot and cold sides, respectively; I_L is the generated load current; R_{in} is the internal electrical resistance of the material.

The generated electrical power is the difference between Q_H and Q_C:

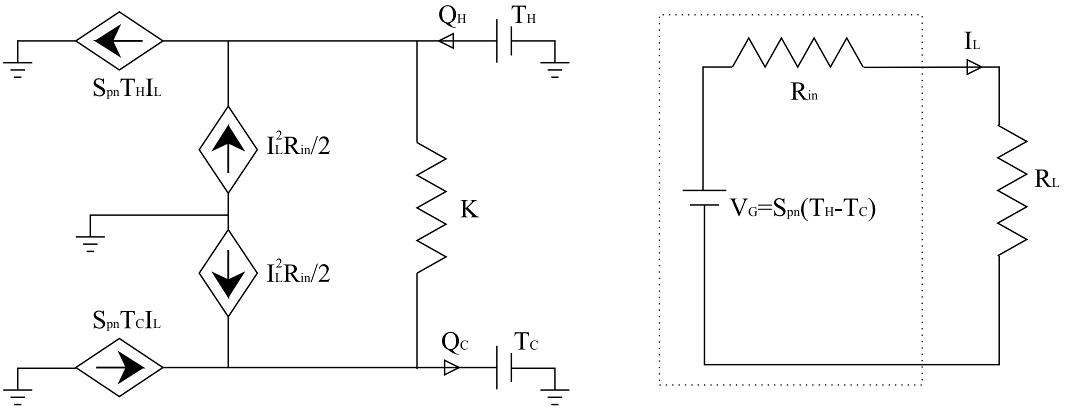
$$\begin{aligned} P_L = &\quad Q_H - Q_L \\ = &\quad S_{pn}\Delta T_{TEG} I_L - I_L^2 R_{in} \end{aligned} \tag{2.9}$$

where ΔT_{TEG} is the temperature difference between the hot and cold sides of the thermocouple.

As seen in Eqn.2.7 - 2.9, besides converting to electrical power, part of the heat power is lost through the thermal conduction and the other part is as Joule heat loss due to the internal electrical resistance, which reduces the power conversion efficiency of the thermocouple. A SPICE model has been built [12, 18] to describe the thermoelectric element electrically, with using the analogies between electrical and thermal variables. Current, voltage and conductance as electrical variables hold the same relation as Q, T and K, therefore, can be used as representation variables in the electrical model of the thermoelectric element, as shown in Fig.2.16(a).

The electrical interface property described by the equivalent Thévenin circuit can be derived from Eqn.2.9, with the internal impedance R_{in} and the open circuit voltage, refer to Fig.2.16(b):

$$P_L = I_L(S_{pn}\Delta T_{TEG} - I_L R_{in}) = I_L(V_G - I_L R_{in}) \tag{2.10}$$



(a) (b)

Fig. 2.16: (a) Equivalent Electrical Model of the Thermoelectric Element; (b) Thévenin Equivalent Circuit

2.3.4 Thermal Energy Harvester Design

2.3.4.1 Performance of the Employed Thermoelectric Generator

Tab.2.5 shows the thermal and electrical data of the commercial thermoelectric generator employed in the test. Fig.2.17 shows the measured matching load resistance R_L changing with the variation of the temperature difference, where the TEG is modelled as a voltage source with an equivalent series resistor (ESR), and the smoothing curve tracking the measured data points is achieved with third-order polynomial fitting. The measurement depicted that the matching load impedance is not constant, but increases slightly with the raising of the temperature difference applied to the TEG pad. The open circuit voltage V_{TEG} increases dramatically with the increase of the temperature difference, which implies the necessity of tuning the duty cycle for various temperature differences.

The similar MPPT method employed for photovoltaic energy harvesting can be used for TEG. For tuning the duty cycle efficiently, it is important to find out the relationship between the temperature difference and the duty cycle of the applied PWM signal. In this design, the output voltage of the boost converter is maintained as 2.7V for charging the supercapacitor. For a boost converter, when its output voltage is a steady value, the duty cycle of the PWM signal linearly depends on its input voltage which is the output voltage of TEG, as shown in Fig.2.18(a). Recall Eqn.2.5, the output voltage of TEG is proportional to the temperature difference, as shown in Fig.2.18(b). Therefore, a linear relationship establishes between the duty cycle and the temperature difference. In the design, the open circuit voltage output of TEG is regularly measured, and based on it, the duty cycle of the PWM signal is tuned for tracking the maximum power point.

Tab. 2.5: Technical Data of Employed Thermoelectric Generator

Parameter	Unit	Value
Dimension	mm X mm	30.0 X 30.0
Seebeck Coefficient S_{pn}	V/K	0.0537
Internal Resistance R_{in}	Ω	3.41
Thermal Conductivity K	W/K	0.312
Maximum Operating Temperature	^0C	150

2.3.4.2 Utilization of Solar Heat

The target application is to supply the power for the sensor nodes which are used for bridge health monitoring. The main heat source of TEG is solar heat. For well utilising the solar heat, exploration on several materials has been done. The thermal properties of the design material of the bridge like stainless steel and brick are examined and sum-

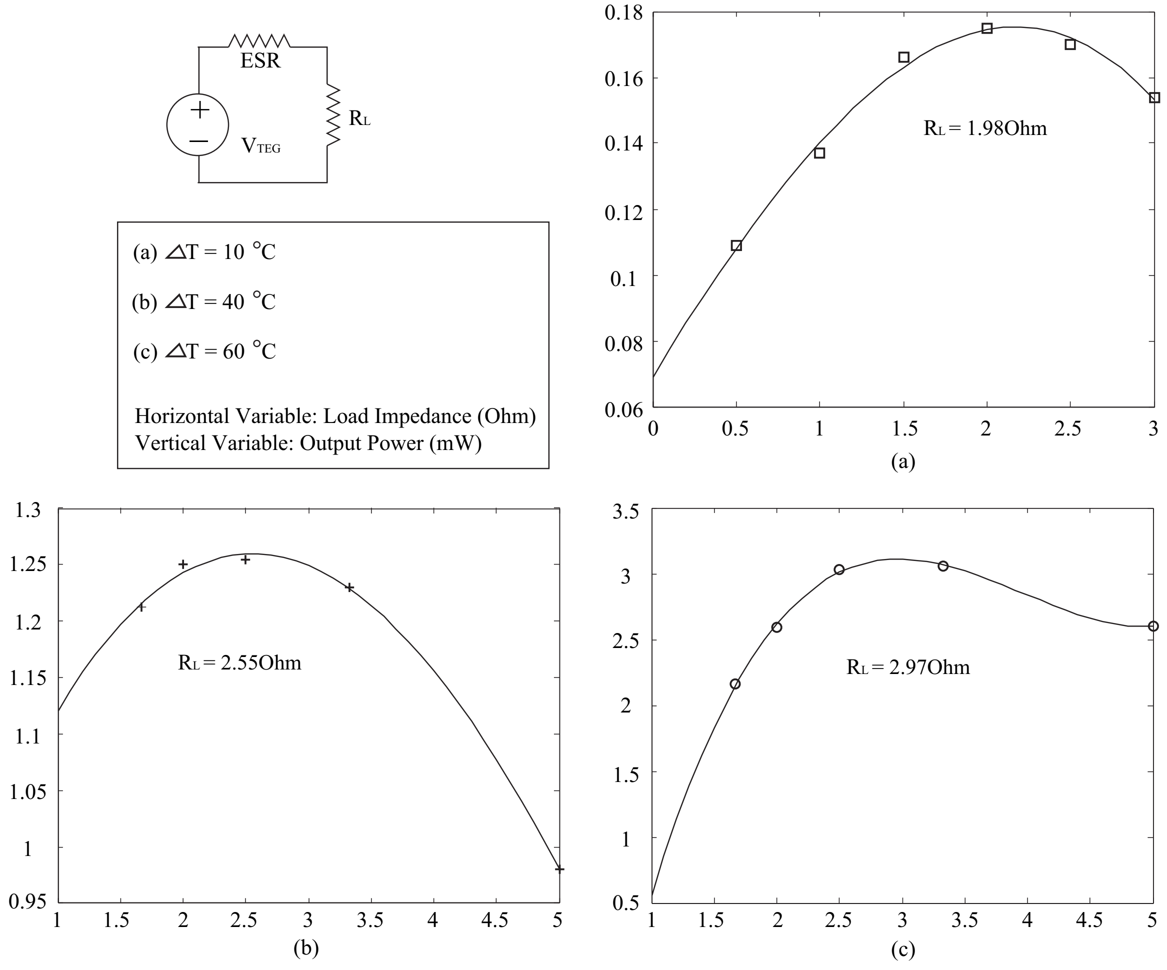


Fig. 2.17: Matching Load Resistance Changes with the Variation of the Temperature Difference

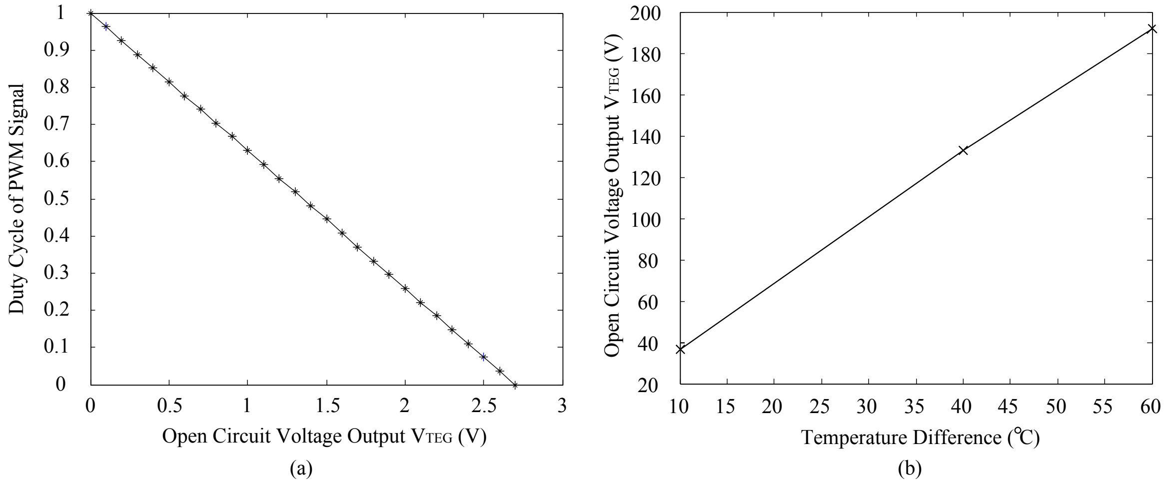


Fig. 2.18: Open Circuit Voltage Output of TEG Depends on Temperature Difference

marised in Tab.2.6.

Stainless steel has a very small heat capacity and when exposed in the sunshine, the temperature of the steel gets high very soon. With a high thermal conductivity, when

Tab. 2.6: Thermal Property of Some Materials

Material	Thermal Conductivity ($Wm^{-1}K^{-1}$)	Heat Capacity ($Jg^{-1}K^{-1}$)
Aluminium	250	0.897
Iron	80	0.45
Water	0.58	4.1813
Soil	1.5	0.8
Stainless Steel	16	$\sim$ 0.5
Brick	0.6-1.0	0.9

the sunshine disappears, the temperature of the steel drops soon. To form the high temperature difference, a material with different thermal property is required. Water is a proper choice for its high capacity and low thermal conductivity that when exposed in the sunshine, the temperature of the water does not rise very soon, and since the heat will be kept in the water and when the sunshine disappears, the temperature does not drop soon. However, attaching a side of the TEG module directly to the water is not feasible. In the test, a cold pack is used instead. By attaching the hot side of the TEG pad to the steel and the cold side of the TEG module to the cold pack, the open circuit voltage of the TEG module is recorded over days, as depicted in Fig.2.20. For comparison, a second setup is constructed by attaching the cold side of the TEG module with a heat sink, and the recorded data is depicted in the same figure. Fig.2.19 shows the experimental setup: the stainless steel is exposed in the sunshine, while the cold pack and heat sink are attached in the other side of the TEG module in the shadow. From the recorded data, it can be seen that, the TEG module of which the cold side is attached by the cold pack results in higher temperature difference than the one attached by the heat sink. Moreover, the cold pack has high heat capacity, and as the sunshine weakens, the temperature of the cold pack

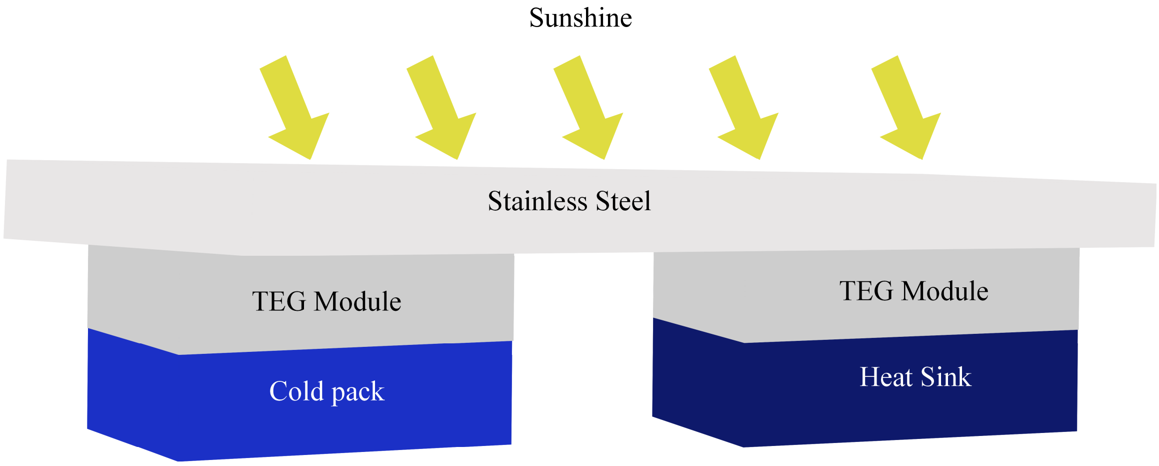


Fig. 2.19: Experimental Setup of TEG Module

drops much more slowly than the steel, which results in a higher temperature in the cold side and hence a negative voltage output. Both heat sinks, which are of aluminium and steel, have smaller heat capacity comparing with the cold pack. For the second setup, the temperature difference between the two sides of the TEG module converges to zero as the sunshine withdraws, and as seen from Fig.2.20, the output voltage of the TEG module is nearly zero.

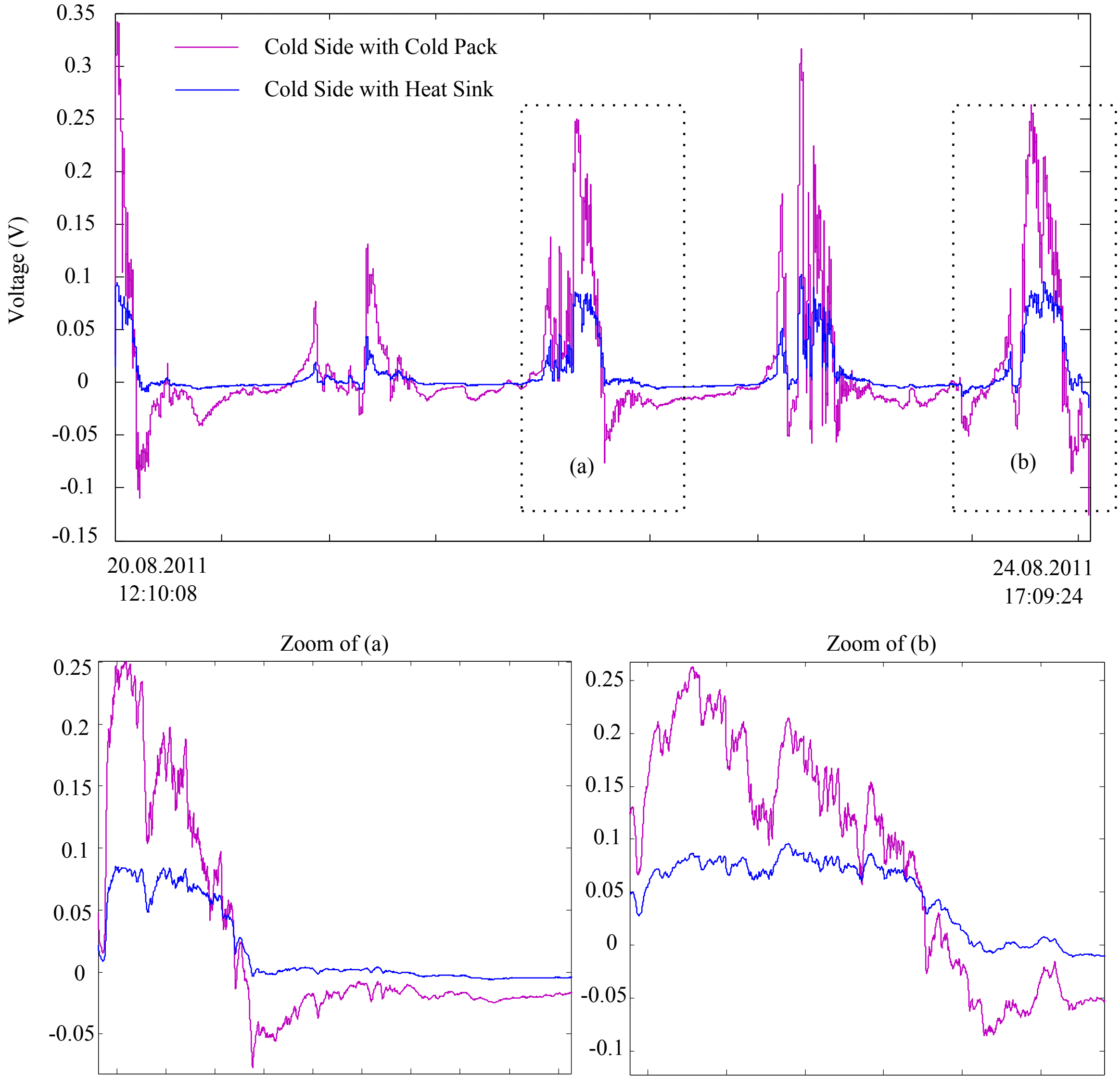


Fig. 2.20: Recorded Voltages of the TEG Module by Attaching the Cold Sides to Cold Pack and Heat Sink

2.3.4.3 Power Management Circuit Design

The above experiment shows that, when using a thermal mass in the cold side, the solar heat is well utilized. The induced voltage from the TEG module changes its polarity as shown in Fig.2.20. Due to the limited voltage amplitude induced from the TEG module, it is suggested to boost the induced voltage to a higher level. A differential common mode DC/DC boost converter can be employed. When the output voltage of TEG module is positive, the positive single-ended circuit is started with a PWM signal generated by the control unit, and the negative single-ended circuit is opened by a second PWM signal with a duty cycle set at 0. When the output voltage of TEG module is negative, the negative single-ended circuit is then started by applying the second PWM signal with a proper duty cycle, and the positive single-ended circuit is opened with setting its PWM signal to 0.

Fig.2.21 shows the block diagram of the designed power management circuit for TEG. The output voltage of the TEG is regularly detected by the controller unit, and the PWM signal generation is stopped once the energy harvested by the TEG is less than the power consumption of generating the PWM signal.

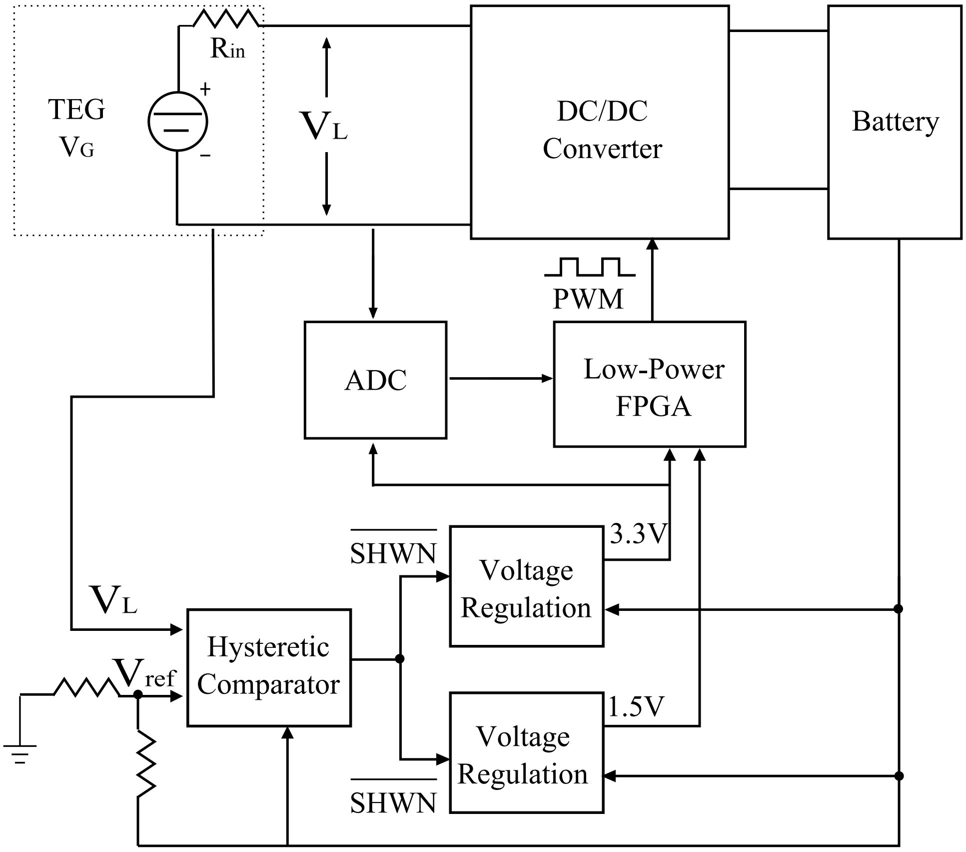


Fig. 2.21: Block Diagram of the Designed Thermal Energy Harvesting Circuit

2.4 Piezoelectric Energy Harvester

2.4.1 Vibration Source

In the environment, there are plenty of vibration sources ranging from human motion to industrial machines. Some existing applications with different vibration sources which have been utilised for energy harvesting are summarized:

- Human Motion: Shenck et al. [62, 103, 104] demonstrated to harvest power from shoes while people are walking with a mounted piezoelectric system. The harvested power is more than 1mW and is sufficient to supply a RFID transponder. González et al. [39] presented the available possible energy sources which can be found in the human body's motion, like breath, blood flow, human walking etc., which can be converted to electricity for charging the wearable devices, like a MP3 player. [78]
- Rolling of Vehicle Tire: Tire Pressure Monitoring System (TPMS) uses a sensor to monitor the air pressure of the tire. To power such a system, a big volume battery is normally employed, and the frequent replacement/recharging of the battery greatly increases the maintenance costs. An approach of realizing the energy self-sustaining, is to harvest the power from the vibration caused by the rolling of the tire with an energy transducer, to continuously charge the battery [54, 89] or even replace the battery [87].
- Car Engine: Applying wireless sensor networks in automobiles is to collect technical data like tire pressure, illumination condition, fuel consumption etc. from a car and provide to the driver for pre-acknowledgement [109]. The vibration of the engine can be used as an energy source to power up the surrounded sensors.

2.4.2 Energy Conversion Mechanism

To convert the mechanical motion/vibration to electrical power, three typical conversion mechanisms can be applied: electromagnetic, electrostatic and piezoelectric. Those methods are originally proposed for sensors or actuators and can be reversely used as electrical energy harvester.

- Electromagnetic power conversion employs an inductor, and with moving the inductor in a magnetic field, current flow will be generated in the inductor.
- Electrostatic power conversion can be illustrated with a parallel plate capacitor, and with moving the two plates relatively to one another, the quantity of the charge over the plates is then changed when the voltage is held constant.
- Piezoelectric uses special material, which physically deform in the presence of an electric field, and such material is usually used for sensors or actuators. Reversely,

> the material can produce electrical charges when physically deformed, and with such a property, the material can be used for energy harvesting by attaching the material in a vibration device. [93]

In the following section, the piezoelectric power conversion will be described, and a design based on this design topology will be presented.

2.4.3 Electrical Model and Interface Property

The circuit model of a piezoelectric element is shown in Fig.2.22. The variables in the mechanical portion: δ_{in} shown as a voltage source, representing the equivalent input stress which is resulted from the mechanical stress; m shown as an inductor, representing the effect of the mass; b_m shown as a resistor, representing the damping coefficient; Y shown as a capacitor, representing the stiffness element; C_p represents the inherent capacitance of the piezoelectric element, for more details about the equivalent circuit, please refer to [94]. Both mechanical and electrical portions of the piezoelectric element are modelled with circuit elements, and the two portions are coupled with a transformer [93]. Based on the model, Kong et al. [58] studied the source impedance characteristics of the piezoelectric element and proved the effectiveness of using resistive impedance as a load for achieving maximum power output when vibration frequency for excitation is around the resonance frequency band of the piezoelectric element.

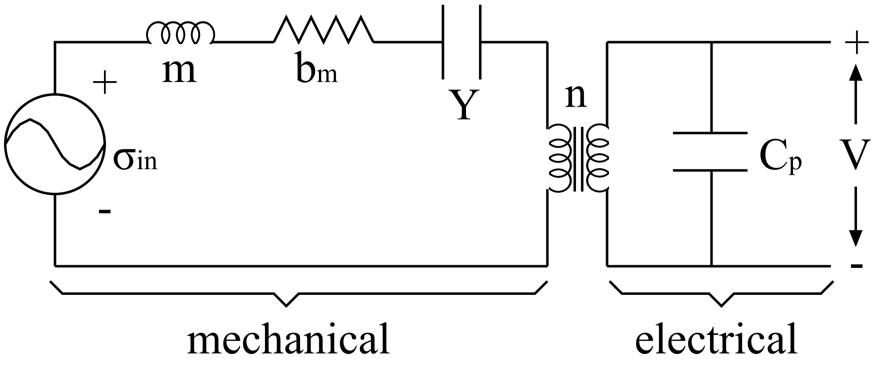


Fig. 2.22: Equivalent Circuit of a Piezoelectric Element [94]

2.4.4 Piezoelectric Energy Harvester Design

2.4.4.1 Performance of the Employed Piezoelectric Element

The following information is provided by Mr. Nader Safi, Fraunhofer-Institut für Betriebsfestigkeit und Systemzuverlässigkeit. The target application is to harvest the power from a vibration absorber which works at a fundamental frequency of 56Hz. A commercial piezoelectric element P-876 DuraAct [86] with a dimension of 61 x 35 x 0,8 mm and electrical Capacitance of 45 nF is used as energy transducer in the experiment. Fig.2.23 shows the experimental setup for measuring the electrical characteristics of the employed piezoelectric element. The piezoelectric element is mounted as a cantilever beam on a bending element. One end of the bending element is fixed to a mass which is used as the vibration absorber. The vibration is stimulated with an electric powered shaker which generates harmonic signal of 56Hz. As the piezoelectric element vibrates, an AC voltage is induced. A full-wave voltage rectifier is connected to the piezoelectric element to convert the induced AC voltage to DC voltage. A variant resistive load is employed for the voltage rectifier. For different applied mechanical strains, the optimal resistive load has been searched for outputting maximum electrical power. The output voltage/power and the optimal resistive load have been recorded and listed in Tab.2.7. The output power is plotted as a function of load resistor, as shown in Fig.2.24, which shows that the optimal resistive load is not a constant value for variant excitation conditions. The piezoelectric element excited with a low-level acceleration requires larger resistive load for maximum electrical power transfer.

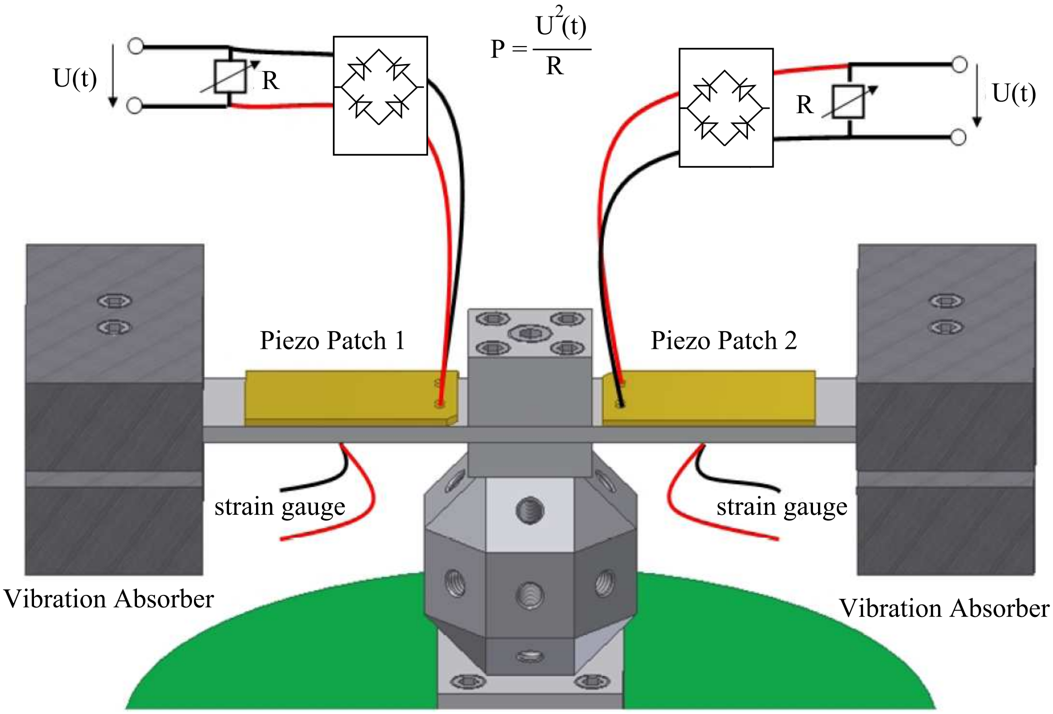


Fig. 2.23: Experimental Setup of the Piezoelectric Power Converter

2.4.4.2 Power Management Circuit Design

The piezoelectric element generates an AC voltage with a frequency depending on the applied excitation stress. A rectifier is usually employed to rectify the AC voltage to a DC voltage. As analysed from the last section, optimal resistive load is not constant but

Tab. 2.7: Optimal Resistive Load Depending on Mechanical Stress

Mechanical Curvature (%)	Base Acceleration Level (g)	Mechanical Stress (N)	Voltage (V)	Optimal Load Impedance (KΩ)	Output Power (mW)
0.0088	2.28	68.29	9.5	75	1.2
0.0163	4.27	136.84	18.8	70	5.05
0.032	9.16	265.72	27.96	45	17.38
0.0473	13.76	395.14	27.33	25	29.88
0.0623	18.18	516.61	28.55	20	40.75
0.0768	22.61	642.74	26.97	15	48.5

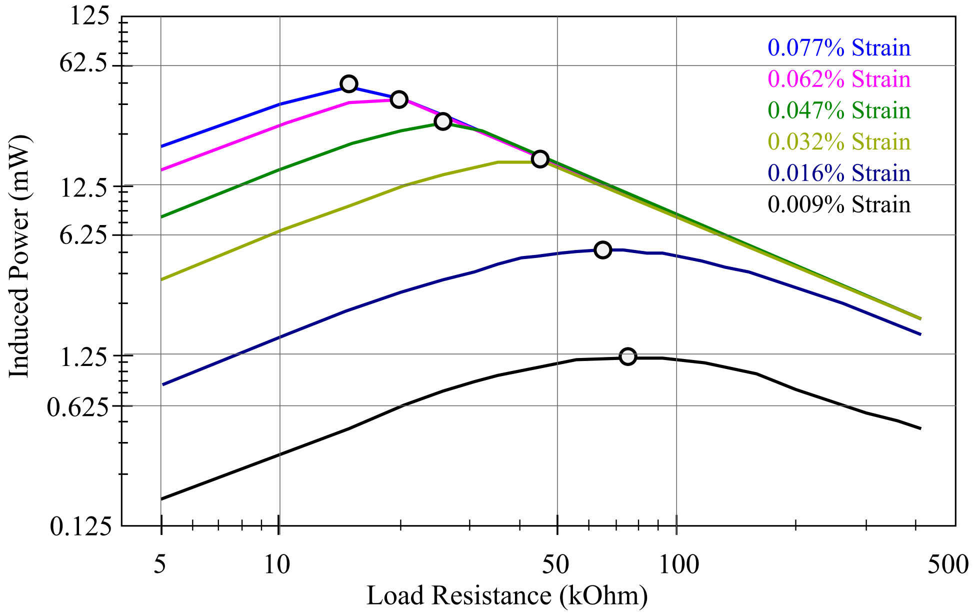


Fig. 2.24: Measured Output Power with Different Resistive Loads

variant accordingly with the applied excitation stress. To achieve the maximum power output in different conditions (different stress levels), an approach, which is similar to the MPPT in photovoltaic energy harvesters [80], can be applied. The designed schematic is shown in Fig.2.25. Considering the measured electrical output characteristics of the piezoelectric element in Tab.2.7, a buck DC/DC converter is employed to convert the rectified voltage to a lower level for further charging the battery. The simulation and experimental results of the designed energy harvester are shown in Fig.4.1, where the presented data is based on the condition: mechanical curvature of 0.0088%, mechanical stress of $68.29N$, please note in Tab.2.7.

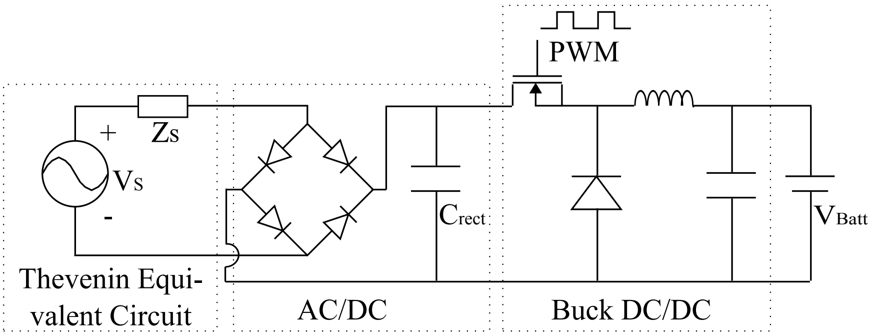


Fig. 2.25: Schematic of Piezoelectric Energy Harvester

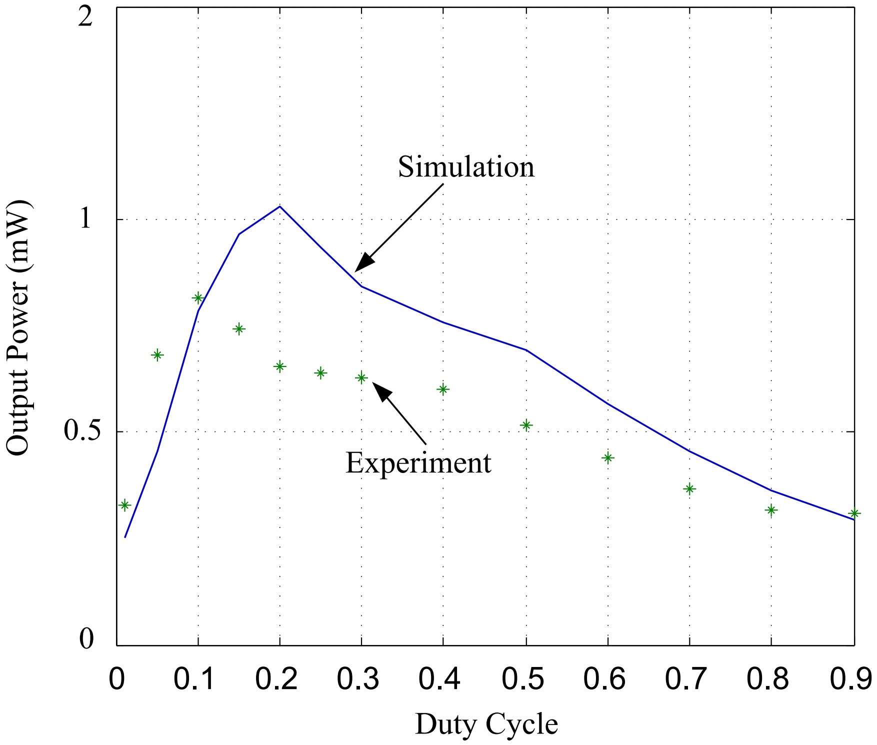


Fig. 2.26: Measured and Simulated Output Power Versus Duty Cycle

2.5 EHS Design and Application in WSNs

2.5.1 General Structure of Hybrid Energy Harvesting System

Electrical energy can be harvested from variant energy sources. Fig.2.27 shows a structure of hybrid energy harvesting system for supplying power for a wireless sensor node, where solar, thermal, vibration and RF energy sources are included. As demonstration, a hybrid energy harvesting system supplying power for HaLOEWEn sensor node is design, where energy is harvested from ambient solar and thermal sources through different transducers: Solar panels and Peltier thermoelectric generators. The harvested energy is stored in a supercapacitor and further transferred to a second storage lithium-ion battery.

To adapt to the changing environment conditions, the maximum power point tracking algorithm is independently implemented for each transducer.

2.5.2 Wireless Sensor Node for Bridge Health Monitoring

The Hardware accelerated Low Energy Wireless Embedded Sensor-Actuator Node (HaLOEWEn) Fig. 2.28 is an advanced modular platform developed in our research group for rapid prototyping of distributed sensing/actuating systems. The platform is built around a low-power FPGA based on non-volatile memory, ideal to use in applications with frequent switches in sleep mode. The sensor node is designed with a low power consumption FPGA, and a Li-battery is used to power up the sensor. To online recharge the battery, an energy harvesting system is designed to harvest power from both sunshine and heat.
The design is for the wireless sensor node application of bridge health monitoring. An application of an advanced wireless sensor node HaLOEWEn is demonstrated. Measurements from an accelerometer are processed by dynamically reconfigurable circuit implemented on a low-power FPGA and a low power RF SoC Microcontroller. Data is wirelessly transmitted to a second sensor node connected to a laptop. A Java GUI allows visualization of the current state of the node and its environment and provides interaction functionalities. The sensor node is powered by a battery recharged by a hybrid energy harvesting circuit. Multiple external sources are used to generate the energy necessary for long term deployments.
For the design of the sensor node, an Actel IGLOO FPGA AGL1000V5 [77] with 1000k equivalent system gates as the central unit of the system has been employed. It is by default extended by a Texas Instruments CC2531 System-on-Chip (SoC), integrating an IEEE 802.15.4 compliant 2.4 GHz transceiver and a 8051 CPU core [110]. The SoC includes 256k programmable Flash memory and 8K RAM. The system runs with a 32 MHz oscillator. Any node can be connected to a PC via the integrated USB port. Through such nodes acting as base stations, data can be accumulated and visualized immediately, and user requests can be disseminated to the whole network. Debuggers can be plugged to the board allowing simultaneous monitoring of the FPGA and the RF SoC operation. The FPGA and the RF SoC communicate via a dedicated SPI bus. When running at the maximum frequency with a DMA controller, data rate can reach 2Mbps. Both components have different deep low power modes, which are useful for applications involving long sleeping periods. The FPGA has a so-called Flash & Freeze Low-Power mode with internal SRAM retention activated by a dedicated pin driven by the software running on the RF SoC. The RF SoC is also able to switch off the power supply of the FPGA, resulting in a deep low power mode with configuration retention since IGLOO FPGAs are based on flash memory. Thus, FPGA functionality is quickly and energy-efficiently recovered after sleeping periods. The power consumption of the FPGA in active mode depends on the implemented design and can range from 4mw to 120mW. When the radio is activated, 47mW have to be added in listening mode and 72mW when transmitting at maximum

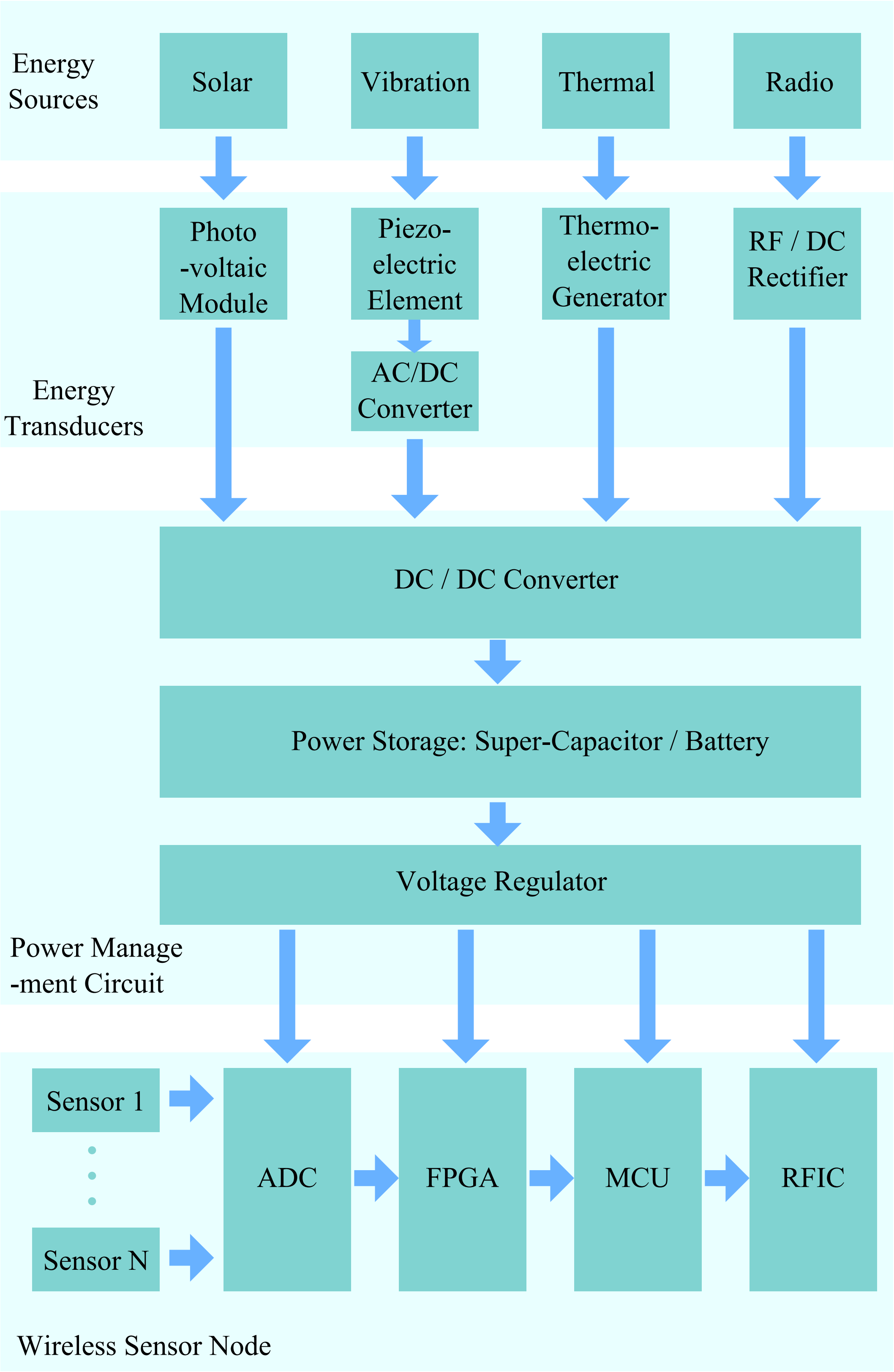


Fig. 2.27: Block Diagram of HEH for Wireless Sensor Node

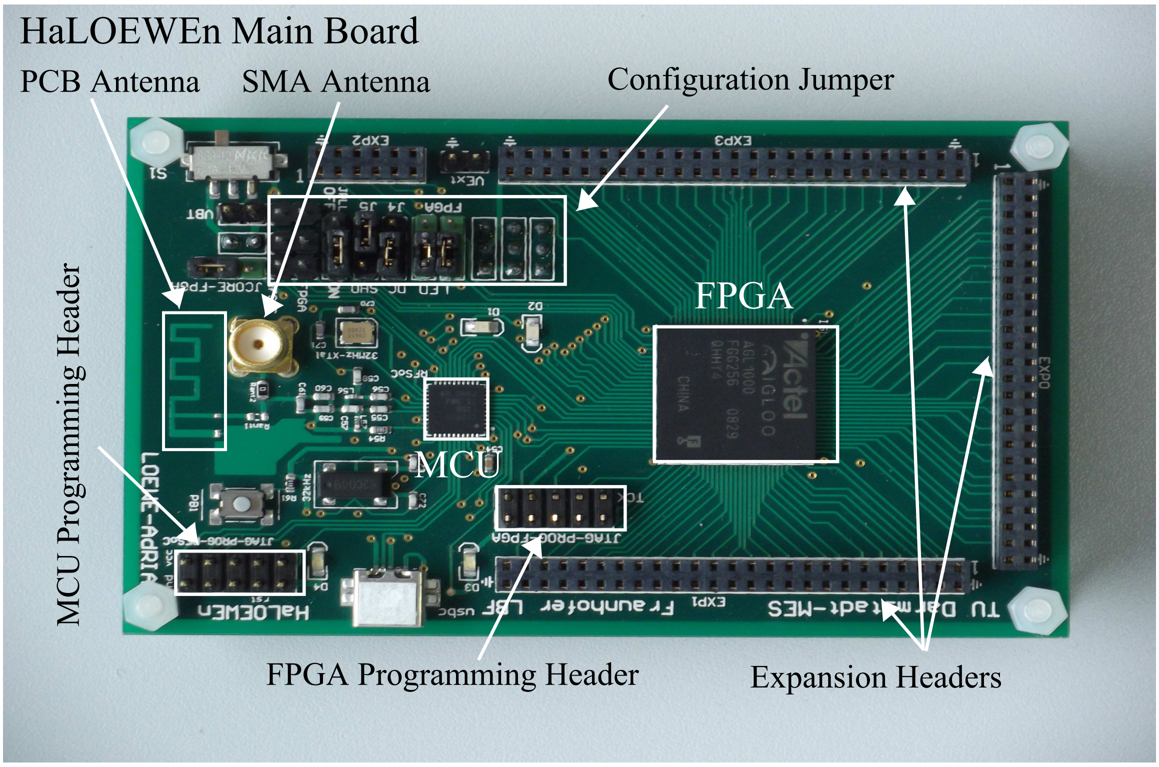


Fig. 2.28: HaLOEWEn-Wireless Sensor Node for Bridge Health Monitoring

power output (10dBm), please refer to Tab.2.8.

The platform can be powered by an external power supply available next to the node or

Tab. 2.8: Power Consumption of HaLOEWEn

Mode	Power Consumption
All active	75mW
FPGA Flash & Freeze - RF SoC Idle	30.7mW
FPGA + RF SoC deep sleep	$50\mu W$

by a battery. If the external conditions are adequate, a hybrid energy harvesting circuit combining power extracted from different sources has been developed for this platform. The latest solutions are well suited for monitoring-only systems, but they are inappropriate when the application includes control of actuators. Power generated by batteries or energy harvesting is not sufficient in this case, and the platform is likely to be supplied by an external source. A temperature and a light sensor were placed by default on the board. Further analog sensors may be attached through an external connector. Other parts of the platforms are customizable modular circuits which are connected to one of the three left FPGA I/O banks. An FPGA with a relatively high number of I/Os (256) has been chosen to maximize the connectivity of the platform. Available extension boards include, for example, additional volatile and non-volatile memory, Analog-to-Digital (ADC) and

Digital-to-Analog (DAC) converters, interfaces to other boards, digital sensors, etc. Each available I/O bank has a dedicated 50 pins header connector to plug the extensions. The board is small enough (60 mm x 96 mm) to be easily integrated in various environments. Accelerometer data captured by the sensor node is pre-processed by the FPGA in order to reduce the wireless communication overhead. Features are extracted from the data by configurable processing stages whose functionality is changed at run time. For maximum power efficiency, resources are shared for different algorithms and programmed in a time-multiplexed fashion.

Data streams are efficiently processed by using dedicated function units and address sequencers. When changing the functionality, new configuration is loaded from an external memory or loaded by the microcontroller and distributed to the different processing elements. For more details about HaLOEWEn sensor node, please note [85].

2.5.3 Hybrid Energy Harvesting System Design for HaLOEWEn

As mentioned, the sensor node HaLOEWEn is designed for monitoring the bridge health. A hybrid energy harvesting system has been developed for HaLOEWEn, with harvesting power from the available ambient energy sources: solar and temperature gradient. Printed circuit board has been fabricated, as shown in Fig.2.29. The hybrid energy harvesting system (HEHS) is to use a low power FPGA (IGLOO-AGLN060V5-VQ100) to generate the PWM control signals for the SEPIC converter of solar cell and the up-converter of thermoelectric generator. Extra triggers are designed to switch off the FPGA when the power consumed by the FPGA itself is larger than the power harvested from the ambient sources. For tracking the maximum power point for the solar cell energy transducer, a power-saving algorithm of ”fractional open-circuit voltage” is applied. The algorithm applies due to the linear relationship between the open-circuit voltage output and the optimal voltage output of the solar cell under varying environmental situations. By periodically setting the duty cycle of the PWM signal to zero, the open-circuit voltage output of the solar cell is sampled by a ADC, and the value is then sent to the FPGA for further determining the optimal duty cycle, by using the look-up table which is designed according to the measured fractional factor.

2.6 RF Energy Harvester

An RF energy harvester consists of the following blocks: antenna, RF-DC converter and a matching network to match the input impedance of the RF-DC converter with the antenna impedance, as shown in Fig.2.31 The RF power source can be either ambient or dedicated, as mentioned in Tab.2.1.

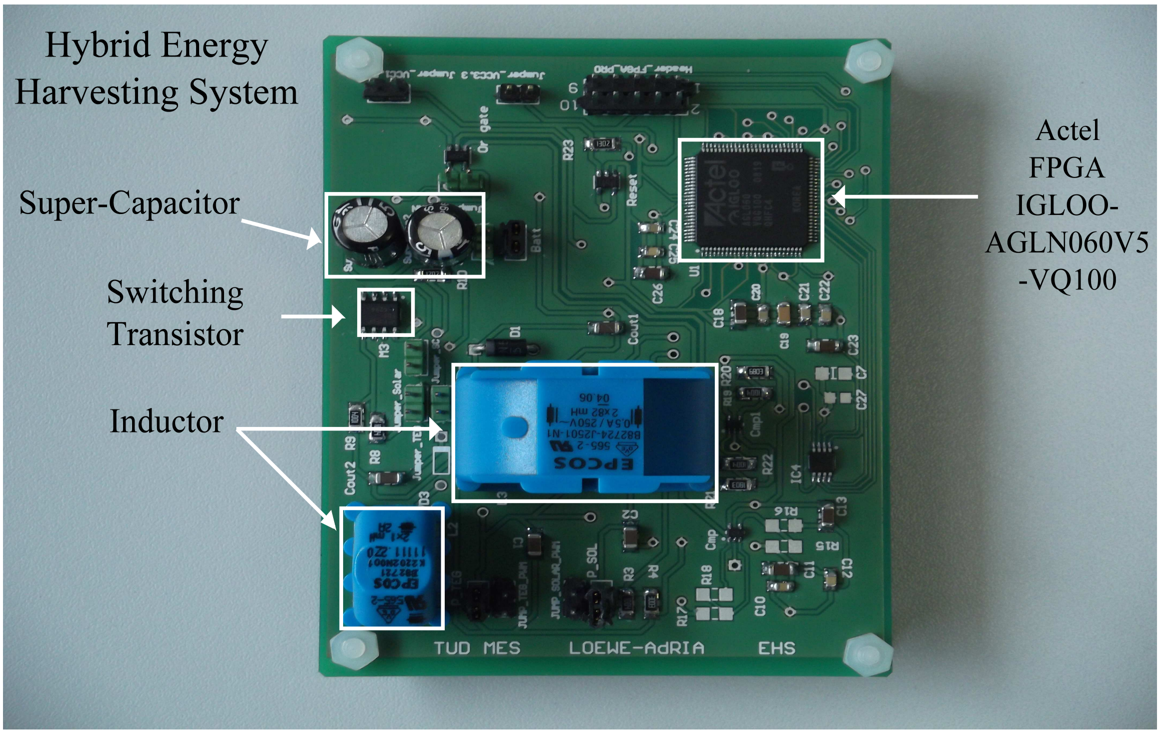


Fig. 2.29: PCB of the designed Hybrid EHS

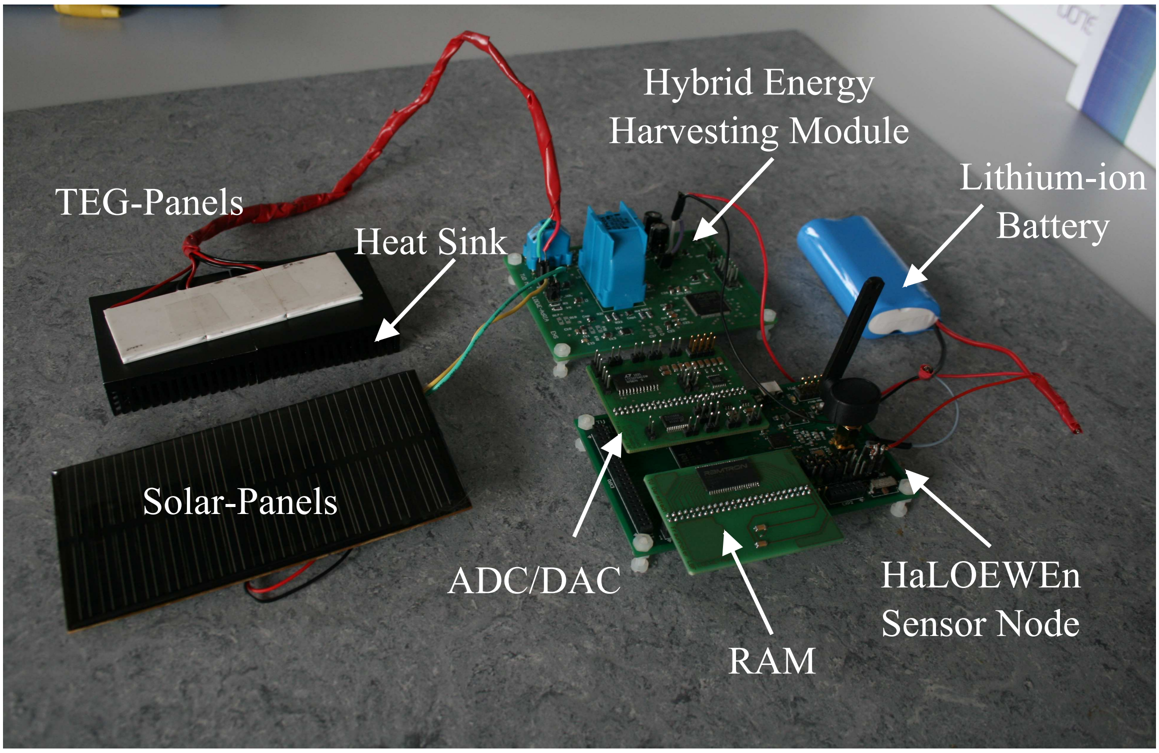


Fig. 2.30: HaLOEWEn with Hybrid Energy Harvesting Module

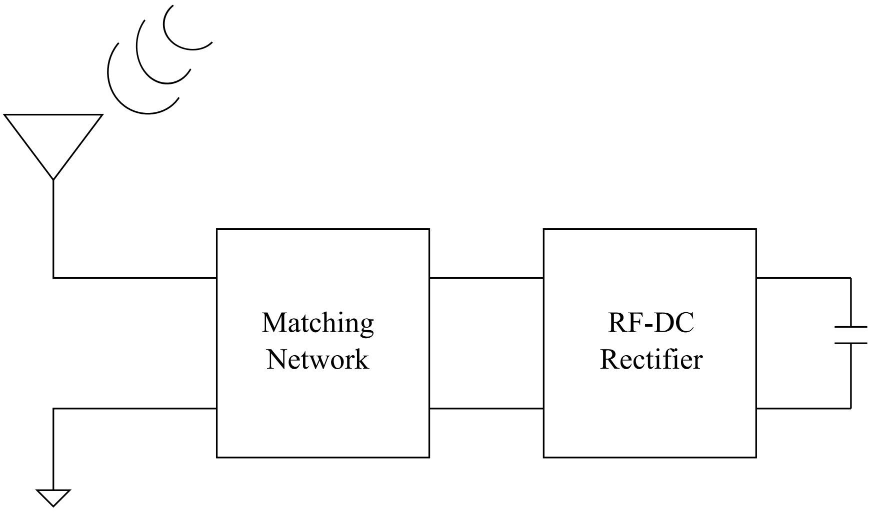


Fig. 2.31: RF Energy Harvester

2.6.1 RF-DC Rectifier Topologies

Different topologies have been developed for RF-DC rectifier design: charge-pump; differential-drive bridge rectifier; gate cross-connected differential-drive bridge rectifier.

2.6.1.1 Charge-Pump Rectifier

Charge-pump rectifier, also called voltage multiplier, as shown in Fig.5.10, has been widely used in micro-power harvesting circuit [7, 10, 52, 102, 114, 126]. The basic structure of the

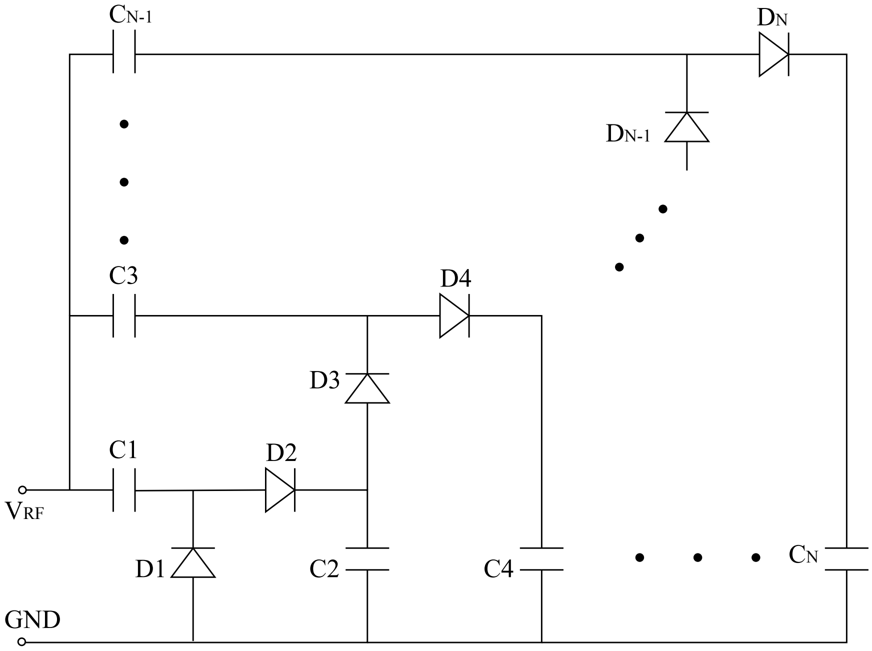


Fig. 2.32: N-Stage Charge-Pump Rectifier

conventionally used charge-pump rectifier is similar to Dickson's DC-DC charge pump architecture [20], which was proposed in 1976 and originally used as DC-DC up-converter. In the RF-DC rectifier application, the circuit is adapted by using the RF input as one of the complementary clock signals, and grounding the other clock line and the DC input line. To understand the operation principle of the rectifier, the first two-stage of the multiplier is considered, which is also usually denoted as voltage doubler. The operation can be analyzed in two cycles: negative half-cycle, when the input RF signal is negative and positive half-cycle, when the input RF signal is positive. Assume the threshold voltage of the diode is V_T and the amplitude of the input RF signal is V_{RF}. In the first negative half-cycle, D1 is conducted, and the charges are transferred to the right end plate of C1. At the end of the first negative half cycle, C1 is charged to $V_{RF} - V_T$. When the positive half-cycle starts, D1 is reverse biased and the right end plate of C1 is pushed to $2 * V_{RF} - V_T$. D2 is turned on, and charges are transferred to C2. At the end of the positive half cycle, C2 is charged to $2 * (V_{RF} - V_T)$. For rectifier with more stage doublers, the DC output of the former stage doubler is used as a DC bias of the following stage.

One of the performance indices for rectifier design is voltage sensitivity, which is defined as the minimum voltage amplitude of the input RF signal required to achieve a certain DC voltage and current at the output of the rectifier [102]. To sense the low induced voltage at the antenna of the receiver which is several meters away from the power transmitter, as in RFID system, a schottky diode with lower potential barrier is preferred [7, 52]. An alternative is to use a MOSFET transistor with an extra threshold voltage cancellation technique to reduce the transistor's turn-on voltage. Umeda et al. [114] proposed a structure for semi-passive RFID tags, in which the gate terminal of the MOSFET is biased with a DC voltage generated by an external battery. To avoid the reliance on the extra battery, Feldengut et al. [33] used auxiliary rectifier to generate the gate bias voltage. To reduce the high reverse leakage current resulted by constant gate biasing, Kotani et al. [59] proposed a differential-drive CMOS rectifier where the gate of the MOSFET is biased by a differential-mode signal. Besides, a gate-drain-connected (diode-connected) MOSFET with low threshold voltage can be used as a diode. Many submicron processes like UMC 0.13-μm provide MOSFET transistors with zero threshold voltage, which can largely improve the voltage sensitivity of the circuit.

Another performance index of the rectifier design is the power conversion efficiency, which is defined as the output DC power over the RF power at the input of the rectifier. A large part of the power is consumed by the rectifier. Generally, the power conversion efficiency depends on many design parameters: load condition, input power level, number of stages, etc. [126, 134]. Considering the first two stages of the voltage multiplier, when D1 is forward conducted, a current flow through D1 and charges C1. The voltage over D1 has the same phase as the current flow through it, and the diode has a resistive loss. When input RF signal is positive, D1 is reversely biased, and for a real diode, a certain amount reverse leakage current flow through the diode, which results in the reverse diode loss. For a certain load condition and a given input power level, to improve the power conversion efficiency, the power loss of the rectifier must be minimized by choosing proper number of stages or transistor size.

2.6.1.2 Differential-Drive Bridge Rectifier

Full wave bridge rectifier, as shown in Fig.2.33(a), has been used commonly in AC-DC voltage conversion. The rectifier has a differential input RF signal. In the positive half cycle of RF signal, diodes D2 and D3 are conducted, while D1 and D4 are reversely biased. In the negative half cycle of the RF signal, diodes D1 and D4 are conducted, while D2 and D3 are reversely biased. In the whole cycle, the load capacitor C1 is charged in a single direction. The DC voltage on C1 can achieve $V_{RF} - 2 * V_{th}$ when the reverse leakage current and other resistive load are considered, where V_{th} is the threshold voltage of the diodes. The circuit starts rectifying once the amplitude of the input AC signal is larger than twice the threshold voltage of the diode, which reduces the voltage sensitivity of the rectifier. To improve the voltage sensitivity, a gate-drain-connected N-type MOSFET or gate-source-connected P-type MOSFET with low threshold voltage can be used instead of the diode, as shown in Fig.2.33(b). To increase the DC voltage level, a stack architecture is applicable by cascading the single cell bridge rectifier in stages with employing coupling capacitors for DC blocking.

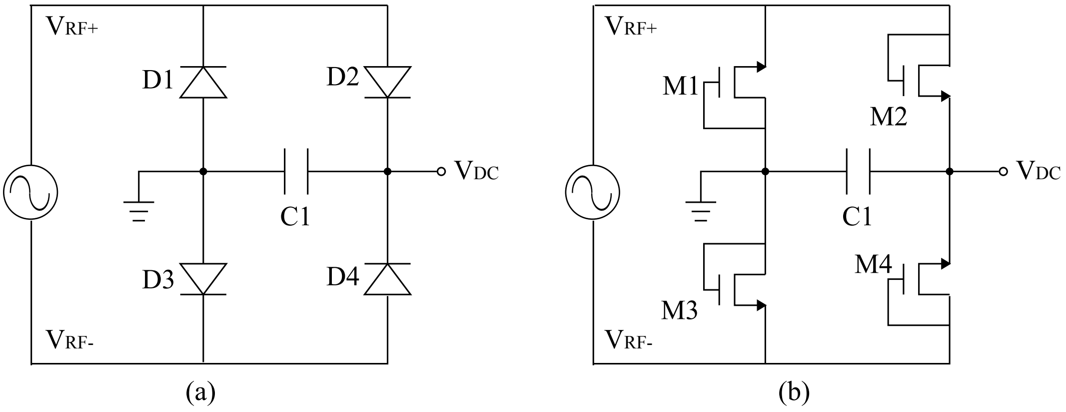


Fig. 2.33: (a) Full Wave Bridge Rectifier (b) Diode-connected NMOS Bridge Rectifier

2.6.1.3 Gate Cross-Connected Differential-Drive Bridge Rectifier

Although by using the diode-connected MOSFET with low threshold voltage, the voltage sensitivity of the bridge rectifier can be effectively improved, the reverse leakage power consumption induced by the MOSFET is not neglectable. An adapted architecture of the conventional bridge rectifier [30, 59, 123] is to bias the gate terminal with the differential input RF signal. With biasing the gate terminal, the turn-on voltage of the MOSFET is reduced, with which, the voltage sensitivity can be effectively improved. Take the architecture in Fig.2.34(a) as an example. In the positive half cycle of the RF signal, as in a normal bridge rectifier, M2 and M3 are conducted, while M1 and M4 are reversely biased.

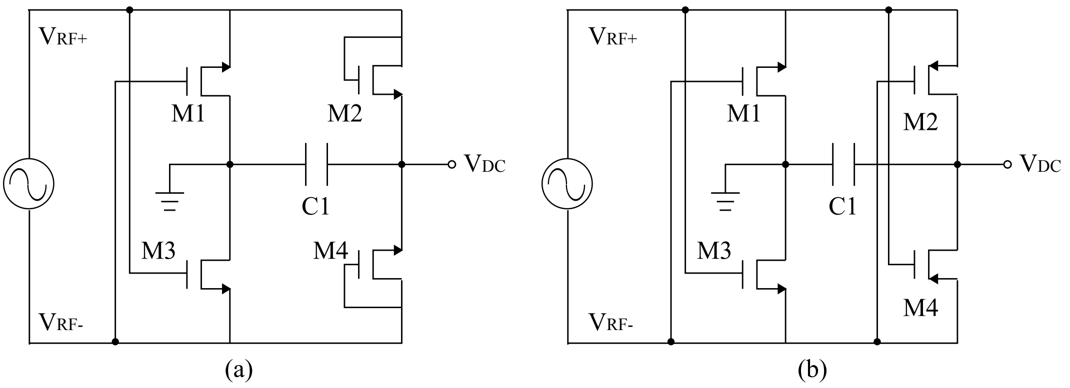


Fig. 2.34: (a) NMOS Gate Cross-Connected Bridge Rectifier (b) CMOS Gate Cross-Connected Bridge Rectifier

The change happens in the bias voltage in the gate terminal of M1 and M3. In the positive half cycle, M3 is conducted with a bias signal larger than 0 (ground potential) as in the conventional bridge rectifier, which reduces the threshold voltage of M3 and hence improves the voltage sensitivity. In the positive half cycle, drain and source terminals of M1 are exchanged. M1 is reverse biased at gate terminal with the negative RF signal, which is lower than the ground potential of the source terminal. With such a bias, the leakage current induced by M1 is largely reduced. The same analysis can be done for the negative half cycle.

In NMOS gate cross-connected bridge rectifier, only two MOSFET are biased differentially. To further improve the performance of the rectifier, two PMOSs are used instead, as shown in Fig.2.34(b). In the positive half cycle, PM2 and NM3 are conducted while NM1 and PM4 are reverse biased. The bias signal at the gate terminal of PM2 is negative, which results in a smaller turn-on voltage than the diode-connected mode. The source and drain terminals of PM4 exchange. The gate terminal of PM4 is biased with the positive RF signal which is larger the potential at its source terminal and hence reduces the reverse leakage current. The same analysis can be done for the negative half cycle.

2.6.2 RF-DC Rectifier Design Element

The commonly used devices for rectifier design are MOSFET and schottky diode. The difference in physical construction results in the dis- and advantages in the application of RF-DC rectifier design. Tab.2.9 summarizes the pros and cons of both devices.

2.7 Summary

In this chapter, the concept energy-autonomous wireless sensor node is presented. Different ambient energy sources: solar, thermal, vibration, RF wave, have been explored, for each, the energy transducer design has been examined. Power management circuits are

Tab. 2.9: Comparison MOSFET and Schottky Diode

Device	Pros	Cons
MOSFET	Standard EEPROM Process Compatible Low threshold voltage < 0.1V	Higher Substrate loss
Schottky Diode	Not Compatible with Standard EEPROM Process High threshold voltage 0.2V $\sim$ 0.3V	Lower substrate loss

designed with employing optimization algorithms to follow the variation of the energy sources caused by the change of the environment. A general concept of hybrid energy harvesting system has been proposed for battery-based sensor node with rechargeable capability. For demonstration, a hybrid energy harvesting system combining thermal and solar energy transducers has been developed for the wireless sensor node which is used for bridge health monitoring. The prototype design can be further extended with integrating other type of energy transducers.

Chapter 3

System-level Analysis, Optimization of the Power Utilization

Contents

3.1 Integration of RFID with WSN

3.1.1 Radio Frequency Identification (RFID)

RFID (Radio Frequency Identification) technologies have been introduced in many application domains in the past 20 years for automatic identification and localization, such as supply chain management, purchasing and distribution logistics, access control, people and animal identification, international container transportation, airport logistics [32] etc.. RFID offers consumers a high level of security, service and comfort. For example, a shopping list for consumers can be created by an intelligent refrigerator and electronically transmitted to the supermarket in the future. Likewise, the company is interested in RFID technology because it helps cope with the growing requirements. Involving this technology does not request any new regulatory requirements. For example, the personal data will not be affected by RFID technology, when it is used in fields such as in-house production, logistics and inventory management. A RFID system basically contains a transponder and a reader. The transponder is a data-carrying device and is located on the subject which is to be identified. The reader is a read or write/read device depending on the design and technology used, and is used to detect the transponders in its interrogation region [35]. In comparison to classical barcode based applications, transponder technologies can operate in environments where optical tagging and reading methods are not very reliable. The wireless read-out of RFID transponders enables the identification and tracking of moving objects, therefore, new real-time oriented process structures can be realised based on this technology. For long range detection, ultra-high/microwave operation frequency is applied to realize the wireless communication between reader and transponder through the electromagnetic field. The transponders can be designed as active, semi-passive or passive. The active transponder employs a battery as its complete energy source to support both microchips's circuitry and RF communication with readers. The transponders continuously broadcasts radio signals to be recognized and tracked by the reader. The semi-passive transponder, also known as battery-assisted passive, uses a small battery to support the digital section. The RF communication is supported by the reader with a constantly emitted RF power. The transponder backscatters a signal by modulating the RF power received from the reader. For low cost applications, the transponder is usually designed to be passive, and no battery is embodied. The RF power from the reader is the only energy source of the transponder. When the transponder locates in the interrogation region of the reader, it draws the power from the RF signal to activate the digital circuitry. After powering up the transponder, the reader keeps emitting the RF signal to support the communication. The comparison of three different types is summarized in Tab 3.1. The reading range of the RFID readers depending on the transmission frequency, the permitted transmission power (ranging from 1mW ERP to 500mW ERP (Equivalent Radiated Power)) as well as the design technology can be up to tens of meters.

3.1.2 Wireless Sensor Networks

Wireless sensor network (WSN) contains a large number of tiny sensor nodes, which are capable of routing the data with a multi-hop technique. With the diverse information provided by the sensor, such as temperature, humidity, blood pressure, acceleration,

Tab. 3.1: Comparison of RFID Transponders [114]

Type	Active Transponder	Semi-passive Transponder	Passive Transponder
Communication distance	Long	Moderate	Short
Necessity of Battery	Need	Need	No need
Cost	High	Moderate	Low

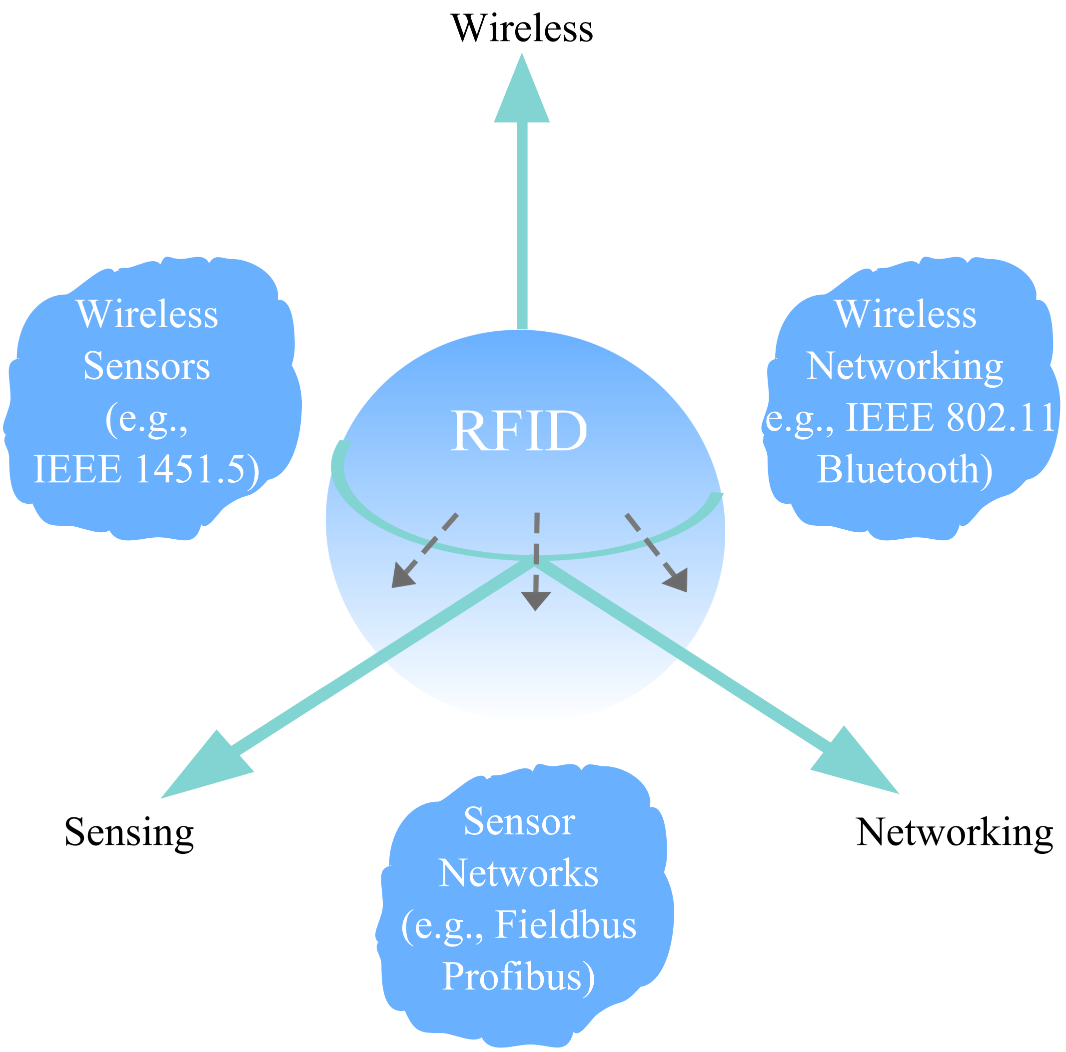


Fig. 3.1: Capabilities of RFID compared with related technologies [8]

vibration etc., wireless sensor network has been deployed in many applications of different areas: structural health monitoring, environment sensing, medical diagnostic/health monitoring, and so on. Since the wireless sensor network supports the multi-hopping mechanism for data transmission, the communication range of the sensor nodes is greatly raised up to hundreds of meters.

Liu et al. [66] has summarized and presented the main difference between the two important wireless technologies, listed in Tab.3.2, which shows that the two technologies complement each other and further indicates the advantages of integrating the two technologies.

Tab. 3.2: Comparison of Wireless Sensor Networks and RFID Systems [66]

Attribute	WSNs	RFID systems
Purpose	Sensing/positioning	Identification/localization
Component	Sensor nodes, relay nodes, sinks	Tags, readers
Protocol	Zigbee (IEEE 802.15.4), Wi-Fi	RFID Standards (ISO/IEC 18000 etc.)
Communication	Multi-hop between sensor nodes	Single-hop between tag and reader
Power supply	Sensor node battery-powered	tag passive/active reader battery-powered/wire-powered
Price	sensor node - medium sink-expensive	Reader - expensive Tag-cheap

3.1.3 Integration Topologies

Several integration technologies have been proposed: in [25], the RFID reader has been integrated in to a sensor network with a microcontroller used for coordinating the two parts, where the RFID reader can exploit the multi-hopping communication provided by the wireless sensor network; Cho et al. [14] has designed an UHF RFID tag chip on which the temperature and photo sensors are integrated for environmental monitoring; similarly, Robinet at el. [91] has developed a remote-powered tag with a capacitive pressure sensor integrated on the same die; Torres et al. [112] validated the integration of an RFID reader to a WSN with the application of identifying the person entering a protected area; Ramamurthy et al. [90] presented a wireless smart sensor platform with an RFID tag integrated on it and multiple radio technologies(Bluetooth, Wi-Fi) for instrumentation and predictive maintenance systems.
From the variant integration technologies, four different topologies of integration have been classified and summarized in [66]:

- Integrating tags with sensors (sensor tags): the RFID tags are expanded with sensing capabilities, and the RFID reader collects information from the sensor tag by using the RFID protocol and single-hop communication. Example designs are remote-powered sensor tag in [91] and tag chip with sensors in [14].

- Integrating tags with wireless sensor nodes: with the integration of RFID tag, the wireless sensor nodes can be expanded with a unique identity number and RFID radio technologies [90]. Some applications reference employed the RFID tag to wake up the sensor node for reducing energy consumption of the node.

- Integrating readers with wireless sensor nodes: the wireless sensor node with a RF transceiver has routing function and can forward information to/from a larger distance over hundred meters, which is far beyond the normal range of RFID readers. Integrating the RFID reader to the wireless sensor node enables the RFID reader working in a multi-hop topology to enlarge the operation area of the reader. Examples can be found in [25] and [130].
- Mix of RFID components and sensors: in this integration, the RFID system and WSN are physically separated, and at the application level, the two systems are integrated with each other at software layer, e.g., the WSN aids the RFID reader to find the location of the specific object with the identification information provided by the RFID system. Representative example design can be found in [13], where a group tour guiding system is presented with WSN used for finding the location of the group leader with the identification of the member provided by the RFID system.

Above integrations show the advantage of combining RFID technologies and WSN. In this work, the topology of integrating RFID reader to a wireless sensor node has been focused with concentrating on reducing the power consumption of the reader for prolonging the battery usage. The architecture of integrating RFID reader with a wireless sensor node has been proposed in [25] and [130], where the platform for the wireless sensor node includes a microcontroller which serves also as a coordinator between sensor node and the RFID reader. In Chapter 2, the wireless sensor node is proposed to be designed with low-power FPGA. The RFID reader can be also FPGA-based [95] for conveniently supporting various protocols, and the FPGA-based RFID reader design will be introduced in the following chapters in detail. Deploying the FPGA-based wireless sensor node and RFID reader, the integration architecture can be designed as shown in Fig. 3.2.

The following sections are organised as follows: in chapter 3.2, the power utilization is analysed based on the proposed architecture which indicates the importance of improving the power utilization of the RFID system and the necessity of employing a novel structure for reader design with automatically tuneable power emission; in chapter 3.3, a SDR based RFID reader architecture is introduced which can easily implement automatically tuneable power emission; in chapter 3.4, the design of the digital core of a transponder is described together with some power saving strategy. The power consumption of individual blocks of the digital core, as well as the power consumption variation over time including both power-up and communication phases is recorded. Based on the power consumption of the transponder, a theoretical analysis on power transmission link from reader to transponder is given. In chapter 3.5, a new structure of reader design is proposed. The difference of the power consumption envelope of passive transponders de-

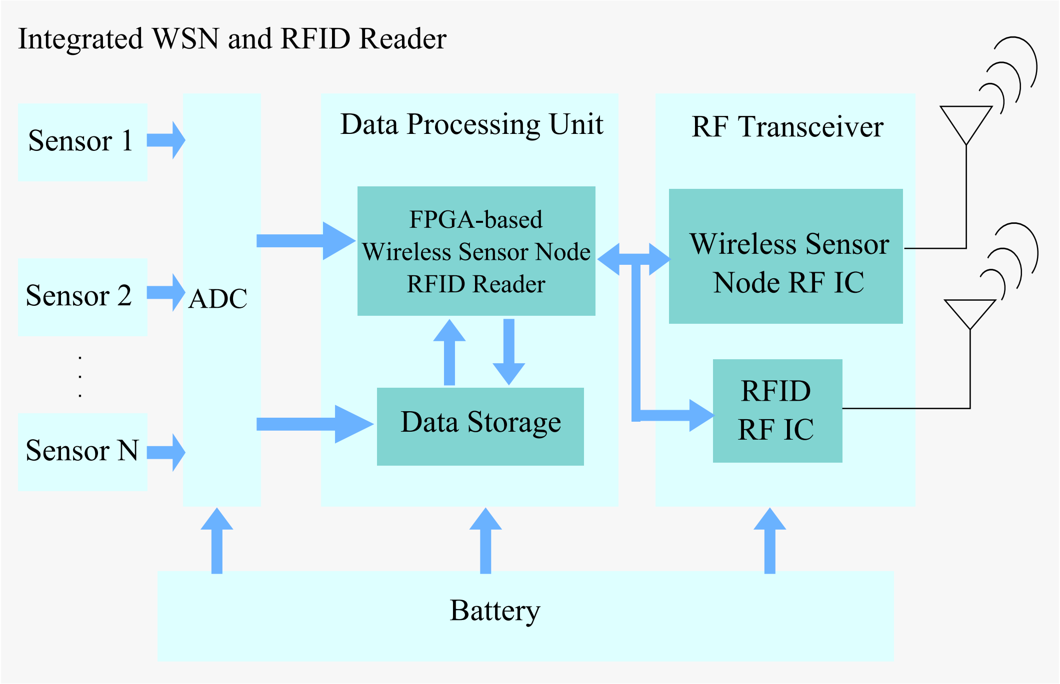


Fig. 3.2: Integration Architecture of Wireless Sensor Node and RFID Reader

signed in compliance with different protocols is considered. The modulation effect of the power control on forward data modulation is also included in the analysis. All numerical data concerning transponder is referred to designs based on UMC 0.13-μm technology.

3.2 Power Utilization of RFID System

The power utilization of the proposed architecture can be estimated. The data processing of the HaLOEWEn platform consumes around 75mW in the active mode, and 50μW at the sleep mode. The supply voltage of the platform is 3.3V, please refer to Tab.2.8. During the communication, the RF transceiver consumes much more power than the data processing part, for around 1W, but the duty cycle of the RF SoC is much less and dependent on the application, here a reasonable value of around 0.01% is assumed. The RFID reader consumes most power during the reading process. For estimation, it is assumed that the reader can be totally shut down when it is in idle mode and consumes no power. Assume a transponder consumes 1μW when being read, the overall power conversion efficiency is 30%, the transmitting signal is at 2.45GHz, and the antenna gain of both reader and transponder is 1. To read a transponder located in 5m, the power radiated by the reader can be calculated with Friis transmission equation, which results in around 0.87W. Assume the wireless sensor node work with a duty cycle of 1%, and reader with 0.067% (read two transponder per minute, each reading process takes 20ms). The average current consumption is:

$$\frac{(1\% * 75mW + 50\mu W + 0.01\% * 1W) + 0.87W * 0.067\%}{3.3V} \approx 0.45mA \tag{3.1}$$

By using a battery with capacity 2000mAh, the life time of the battery to supply such a platform is 0.51 year. The power consumed by the reader is 39.2% of the total power consumption. Therefore, it is important to improve the power utilization of the RFID reader to prolong the battery life.

In passive far-field UHF/microwave RFID transponders, a power harvesting circuit is employed for converting a part of the collected RF power to DC power supply voltage. The input resistance changes greatly with the variation of the load current consumption. In the case where load current is not constant, the matching network is usually designed for matching the input impedance when the load current is maximum [17], and the received power has to be larger than the maximum power sensitivity for obtaining a maximum load current. However, an optimal matching network between the antenna and the power harvesting circuit for one load cannot realize maximum power transfer for other loads, but results in large return loss and hence bad power transfer efficiency [139]. Instead of having a constant power level on the reader side for generating a maximum load current in the transponder, a large amount of power will be saved, if the transmitted power can be tuned according to the needs of the transponder.

In existing RFID systems based on SDR, the emission power of the reader can be controlled according to different standard definitions. Furthermore, in some RFID systems [111], the emission power of the reader is not constant but increases for some command, e.g., "write transponder". The writing operation of transponder consumes more power, and to fulfill the needs of the transponder, the power emission of the reader is adjusted to a higher level.

In fact, the power consumption of the transponder not only varies for one specific operation, but also changes strongly during the execution of all commands. With a maximum constant power emission from the reader during the execution of one command, a lot of power is wasted, which reduces a mobile reader's battery life time and may cause overshoot and reader interference.

3.3 Software Defined Radio Based RFID Reader

Various RFID air interface standards are defined for different target applications, e.g., a series of RFID air interface standards by ISO/IEC from 18000-1 to 18000-7 for the item identification world. A diversity of RFID specifications is regulated. Several frequency bands have been assigned to RFID applications, such as 125KHz, 13.56MHz, 433MHz, 868MHz, 915MHz and 2.45GHz. Each frequency band has an individual parameter definition: modulation/demodulation, encoding/decoding etc., as shown in Tab.3.3. To support various transponders, which are designed in compliance with different standards, flexible multi-range readers are needed. Software Defined Radio (SDR) is a possible solution to realize a multi-protocol RFID reader.

The Software defined Radio (SDR) is not a new concept; the military and cell phone services have considered and used it for many years, because both of them must serve a wide variety of changing radio protocols in real time. Many components of the designed RFID reader system, which are typically implemented in hardware (e.g., encoder/decoder, modulators/demodulators, detectors etc.), are implemented in software.

Tab. 3.3: Link parameters and anti-collision algorithms

Protocol	Forward Link		Return Link		Anti-Collision
	Modulation	Baseband coding	Modulation	Baseband coding	
ISO/IEC 18000-4 Mode 1	ASK	Manchester	ASK	FM0 (Bi-Phase Space)	Randomising the repetition time
ISO/IEC 18000-6 Type A	ASK	PIE	ASK	FM0	Dynamic framed slotted ALOHA
ISO/IEC 18000-6 Type B	ASK	Manchester	ASK	FM0	Binary Tree slotted ALOHA
ISO/IEC 15963 /18000-3 Mode 1	ASK	1 out 4/256 PPM	ASK	Manchester	Dynamic framed

Industry has applied SDR technologies to RFID systems [37, 111]. With employing SDR, several parameters can be reconfigured: operation frequency, modulation scheme, air protocol, transmitted power.

The design philosophy of the SDR RFID, which supports multi-frequencies, multi-protocols and automatic power control, is explained in this chapter. A successful communication system always bases on three principles [99]:

- Modularity, i.e., the abstraction of the larger system into smaller, self-contained subsystems, each with clearly defined behaviours and boundaries;
- Standardization, i.e., the construction of a broad agreement on architectures, module definitions, interface definitions, languages and protocols;
- Renewal, i.e., the ability and willingness to adopt improvements in technology and architecture as they become available in a new environment.

These principles can yield benefits such as: the designs are made easier and clearer, more components are reusable, and most importantly, they are suitable for the large project design and extension for the gradual evolution of technology [95]. In this work, a RFID reader, in which the most functions are done in software (Software Defined Radio), is going to be designed. It supports multi-frequencies, multi-protocols and automatic power control (Standardization), bases on modular design (Modularity), and can be extended easily by adding new features into software component (Renewal). The design is realized on Xilinx XUPV2P board, using the principle of SDR.

Besides the common factors, the other factors are also encapsulated into modules, because the modularity of the RFID reader system enables co-existing of many functions and makes the renewal possibly and easily. For example if the software is expected to read a tag under protocol EPC Class-1 Generation 2 [26], only a small incremental module needs to be added to the software in order to link the protocol and necessary modules, because all required function-blocks are already existed in software database.

The implementation of such a SDR reader, which supports multi-frequencies, multi-protocols and automatic power control, will be detailed explained in the next chapter.

In this work, a multi-protocol reader architecture for UHF and microwave RFID systems is proposed, as shown in Fig.3.3. The software and hardware architecture of the multi-protocol RFID reader is shown in Fig.3.4. The control of frequency, modulation schemes, power emission are implemented with a software defined radio technique. Currently the digital frontend is implemented based on FPGA, and the RF part is simulated with Matlab Simulink, see Fig.3.5. The current version of SDR RFID reader supports ISO/IEC 18000-4 Mode 1 at 2.45 GHz, ISO/IEC 18000-6 Type A and B at 860-960 MHz and ISO/IEC 15693/18000-3 Mode 1 at 13.56 MHz; therefore, it is a platform of standardization. After assembling, encoding and modulation of the command according to the protocol definition, the digital frontend of RFID reader sends data frames (which are finally delivered to the tags) to the analog frontend of the reader. Two control signals are sent out individually to set carrier frequency and power density of sending. The responses of the tags which are received by the analog frontend of the reader will be demodulated and decoded. The information of the valid responses is then redirected to the remote PC via network.

3.4 Power Consumption of Passive Transponders

In passive far-field UHF/microwave RFID transponders, a power harvesting circuit is employed for converting a part of the collected RF power to DC power supply voltage. The transponder has different operations based on the received commands, i.e., compare, read/write memory, idle [46, 47], and the current consumption is not constant but varies over time with respect to different operations. The impedance which is seen from the input of the power harvesting circuit varies with the change of the consumption current of the transponder. Therefore, an optimal matching network between the antenna and the power harvesting circuit for one operation cannot realize maximum power transfer for other operations.

The research is continued with investigating the power consumption variation of the transponder over time for different operation status, and theoretically evaluating the

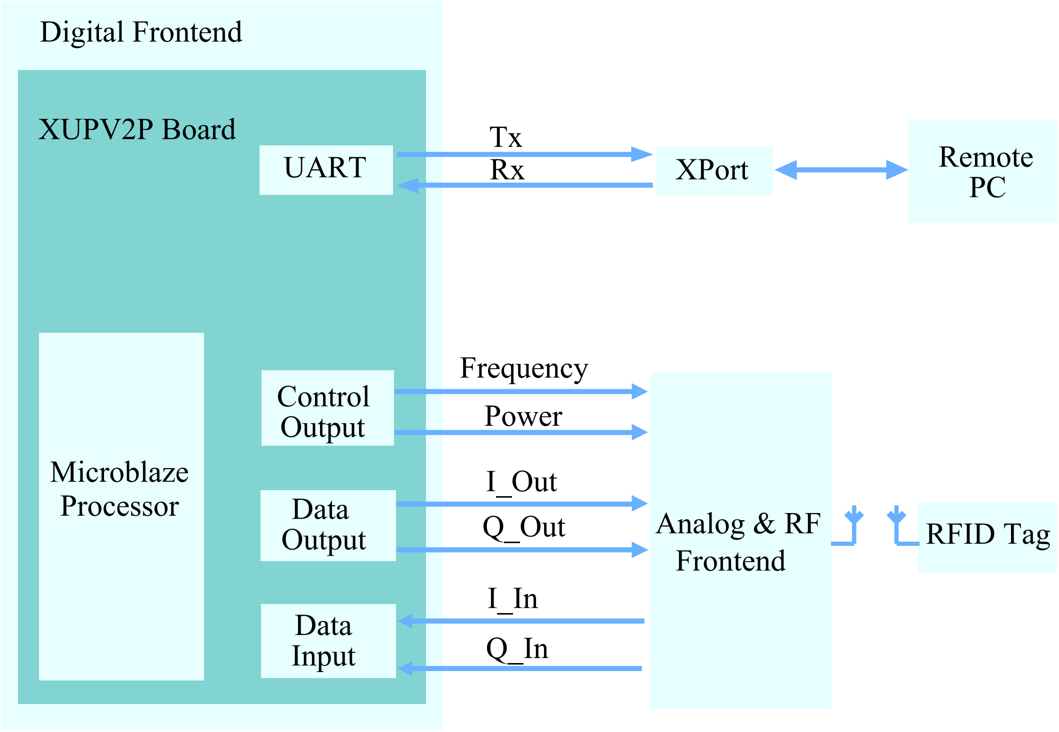


Fig. 3.3: SDR Based RFID System

power saving with employing the automatic tuneable matching network. In this work, the digital section of transponder was developed in compliance with ISO 18000-4/6 [46, 47] and the Faraday low-leakage standard cell library based on UMC 0.13-μm technology was used to synthesize the designed circuit. The power consumption of the designed circuit is estimated with Synopsys PrimeTime, aiming to examine the power consumption variation of the digital section in real time. The architecture of the power supply section of a passive transponder is shown in Fig.3.6. Passive transponders usually employ a voltage rectifier to convert the RF signal to a DC signal as power supply. The output voltage of the rectifier can change strongly according to the change of the input power as well as the load current consumption. Therefore, a voltage regulator is used to regulate the rectifier output by comparing with a stable voltage reference. After the output voltage of the regulator achieves a desired value, an increase of the rectifier output voltage will be observed when the load current consumption drops, even with a stable power at the rectifier input. In order to avoid voltage overdrive, the normal method is to employ a voltage limiter which provides a bypass path for rectifier's direct current (DC) to flow through [5,16].

Besides, a large storage capacitor is necessary to work as the on-chip battery when very low power is available at the transponder due to the forward and backward modulation [5]. From this point of view, a large capacitor is preferred to keep the supply voltage stable even when the load current is large. However, large capacitor means large chip area and consequently high cost. A small storage capacitor makes the modulation with large depth difficult especially when the load current is big. These aspects lead to a trade-

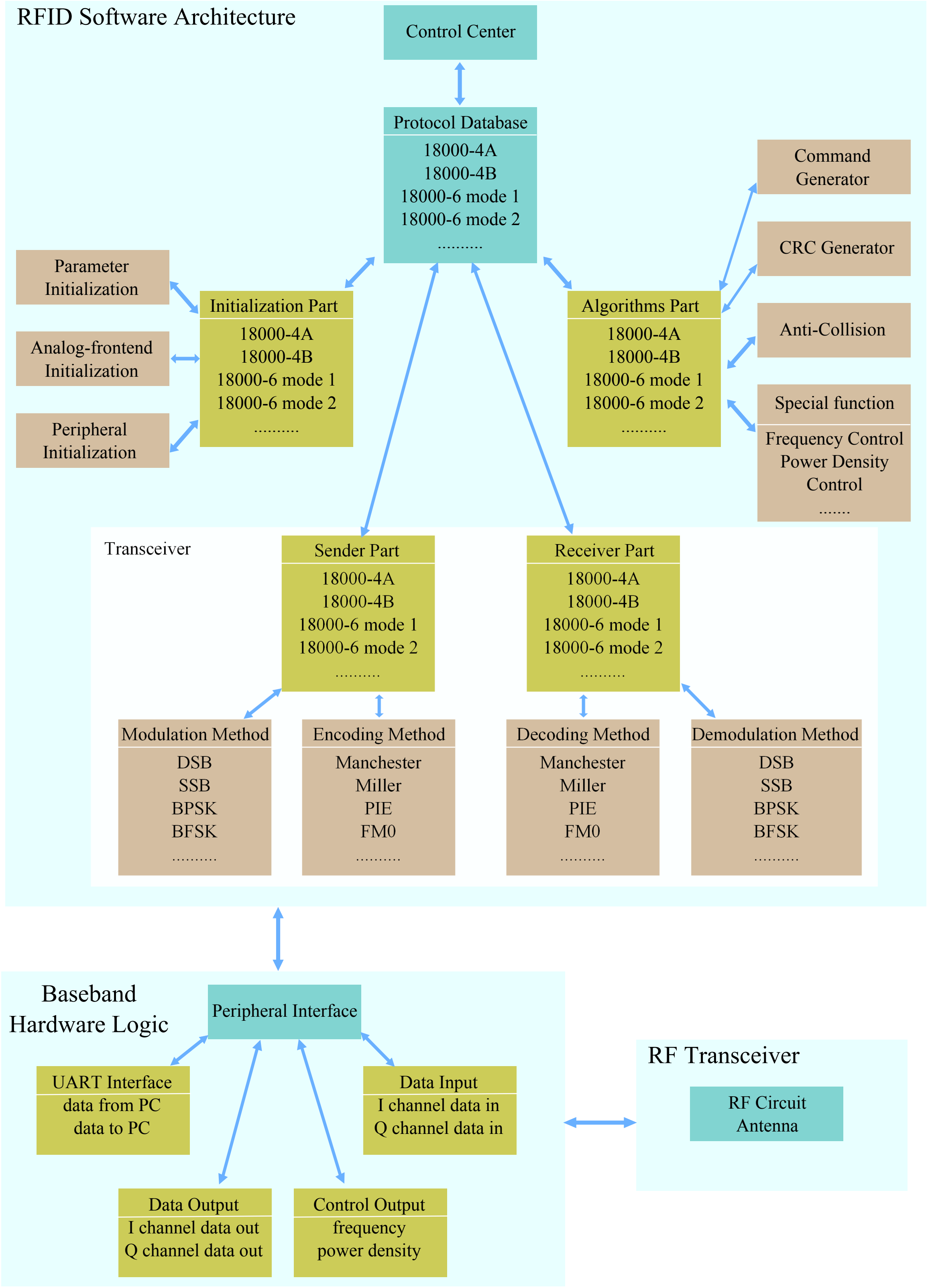


Fig. 3.4: Software and Hardware Architecture of the Multi-Protocol RFID Reader

off for choosing the storage capacitor.

Now the operation of passive RFID transponders is to be considered. The analysis is

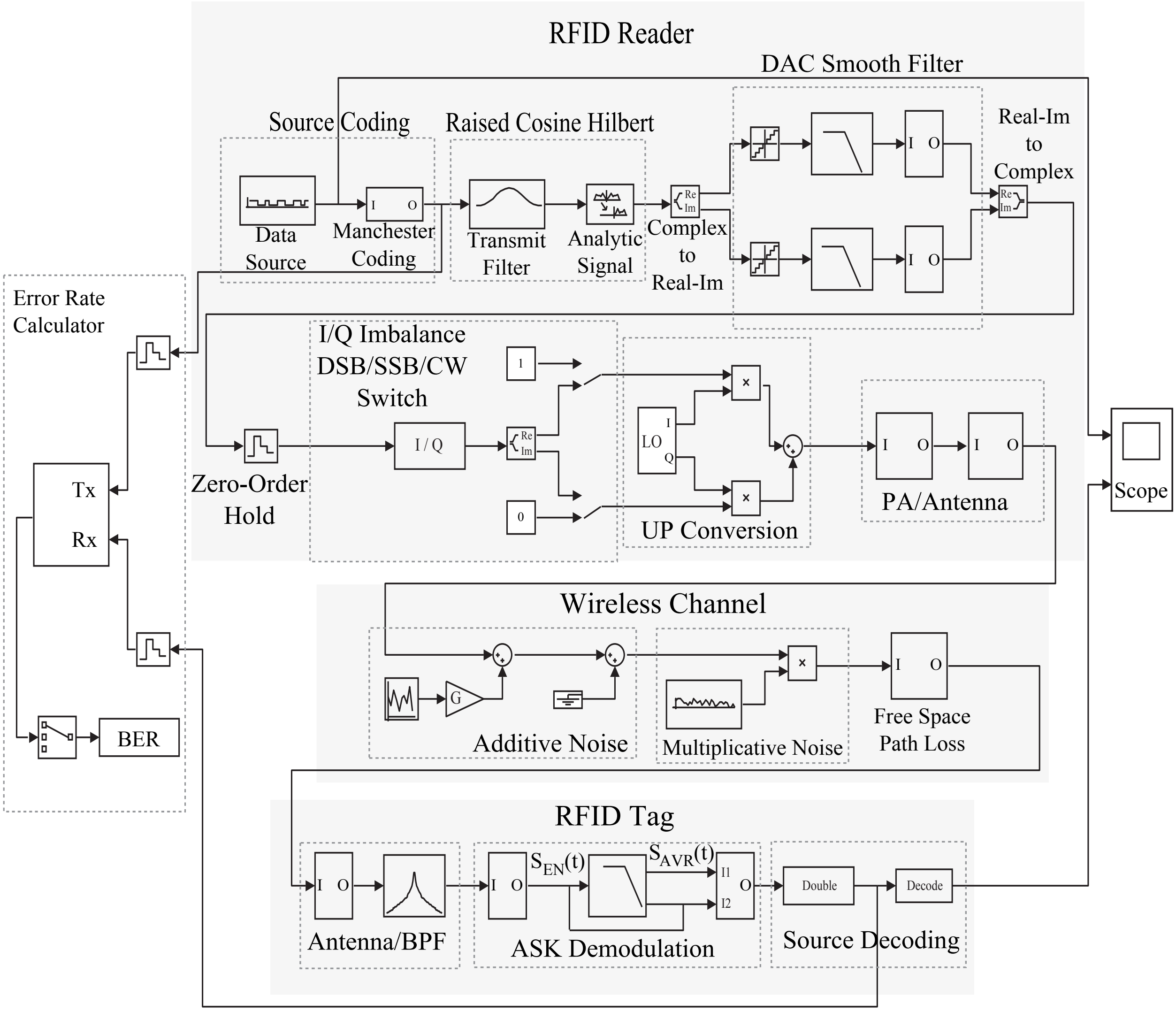


Fig. 3.5: Forward Link Communication in Matlab Simulink

divided into two phases: power-up and communication phase. In power-up phase, the reader sends a continuous wave to the passive transponder to charge up the load capacitor to a certain desired voltage level; after the first phase, the reader starts to send data to the transponder and the communication phase begins. Now the power consumption of the transponder in these two phases is to be analyzed separately.

3.4.1 Power-Up Phase

During the power-up process, no data are received, and the digital section of transponder does not work. Therefore, very little power is consumed by the digital part of the transponder. The load current of the rectifier mainly charges the storage capacitor to the desired voltage level. The current is neither small nor constant. The reader starts with an initial emission power level to power up the transponder. When the regulated voltage achieves the desired value at transponder, the charge current (output current of

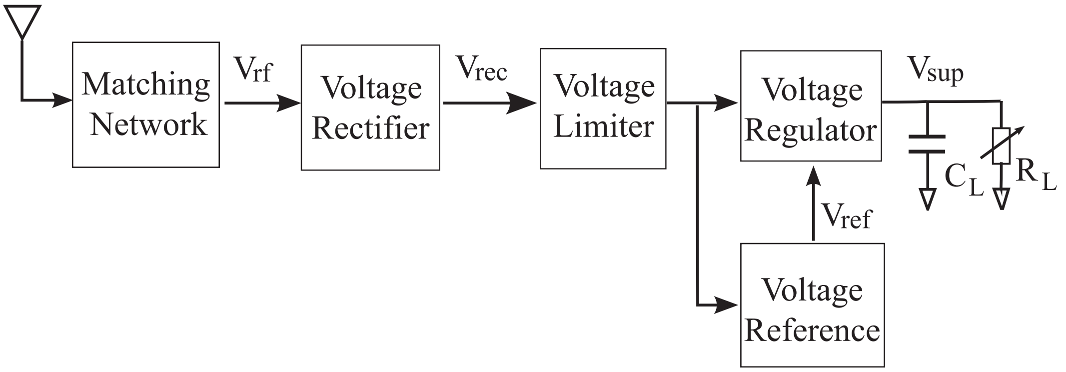


Fig. 3.6: Power Supply Section of Passive Transponder

rectifier/current flowing through the pass transistor) drops dramatically, and the output voltage of the rectifier increases correspondingly. The voltage limiter starts to work to bypass the direct current in order to keep the rectifier voltage in a certain range. However, large amount of power is wasted by bypassing the current. Moreover, in spite of the fixed charging time defined by protocols [46,47], the required time for charging the regulator output voltage to the desired value is uncertain. It depends on the size of the pass transistor of the regulator, the value of load capacitor and the available input power at rectifier. Currently, available standards do not allow the talk between reader and transponder during the charging time. In case that the transponder is powered up before the defined time, the remaining power will be wasted by bypassing the current.

For example, the output supply voltage V_{sup} is set at 1V, which is a reasonable value for the applied technology. The maximum current consumption of the chip is set as 5μA, and the equivalent load impedance R_L is 200KΩ. For 100$\%$ ASK modulation depth and to keep the supply voltage stable, the discharge time $R_L * C_L$ must be at least 10 times as the signal '0' period, which in this calculation has a value of 12.5μs [46,47]. This results in a storage capacitor C_L of 625pF. The pass transistor of the LDO (low dropout) regulator is designed with a size W/L equal $5\mu m/0.12\mu m$. The simplified circuit is shown in Fig.3.7.

Two simulations are executed: in the first one, a continuous wave with constant envelope is sent to rectifier; in the second one, the RF signal amplitude is reduced by 20% after the supply voltage achieves 1V, and the results are shown in Fig.3.8 and Fig.3.9, correspondingly. As it can be seen from the simulation results, without power control, after the regulated voltage V_{sup} achieves the desired supply voltage 1V, the current flow to the storage capacitor I_C starts to drop dramatically, and the output voltage of rectifier V_{rec} increases greatly. If a voltage limiter is applied, V_{rec} will be brought down by bypassing the extra charges. In the second simulation, the input power of the rectifier is changed to a lower level once the regulated voltage V_{sup} achieves the desired value, and the output voltage of rectifier V_{rec} is brought down without applying voltage limiter.

Now it is an open question how to make the reader cognize the completion of power-up phase, such that it could change the emission power level. A backward talk is assumed to be executed. If the change of the charge current can trigger a feedback signal to the reader,

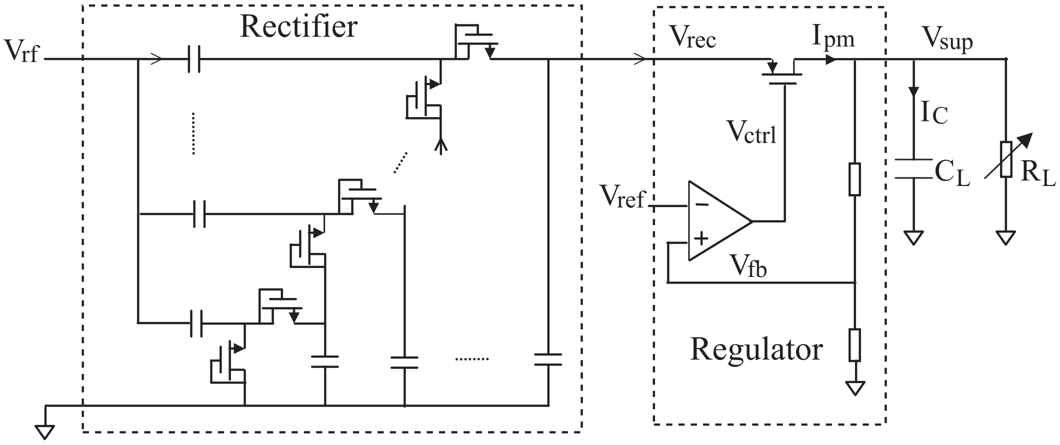


Fig. 3.7: Simplified Power Harvesting and Voltage Regulation Circuit. The voltage divider in regulation circuit employs resistors with high value, and the current flowing through it can be ignored compared to the load current.

with which reader knows the power up phase is done, the reader can emit less power or start the communication phase. Assuming a single tag scenario in which the transponder is not moving, with the charging time and known transponder circuit properties, the reader can evaluate the distance to the transponder and further decide how much power it needs to emit for the communication phase.

3.4.2 Communication Phase

After the communication phase started, the power consumed by the transponder is not constant neither. The transponder has different operations based on the received commands, i.e., compare, read/write memory, idle [46, 47], with which different function blocks in the transponder, e.g., comparator, memory, CRC (Cyclic Redundancy Check) etc., are enabled. Therefore, the current consumption varies over time and the received commands.

In this work, a methodology of real-time operation-dependent power consumption analysis for passive transponders was proposed with classifying the command sets. The digital section of a passive transponder was designed in compliance with ISO/IEC 18000-4/6 using a Faraday low leakage library based on the UMC 0.13-μm technology. The power consumption of the transponder was estimated under different operations with Synopsys Primetime, considering both static and dynamic power consumption. Simulations were done to investigate the power consumption variation over time.

3.4.2.1 Design of RFID Transponders

ISO/IEC defines a series of RFID air interface standards from 18000-1 to 18000-7 for the item identification world. A diversity of RFID specifications is regulated. Several fre-

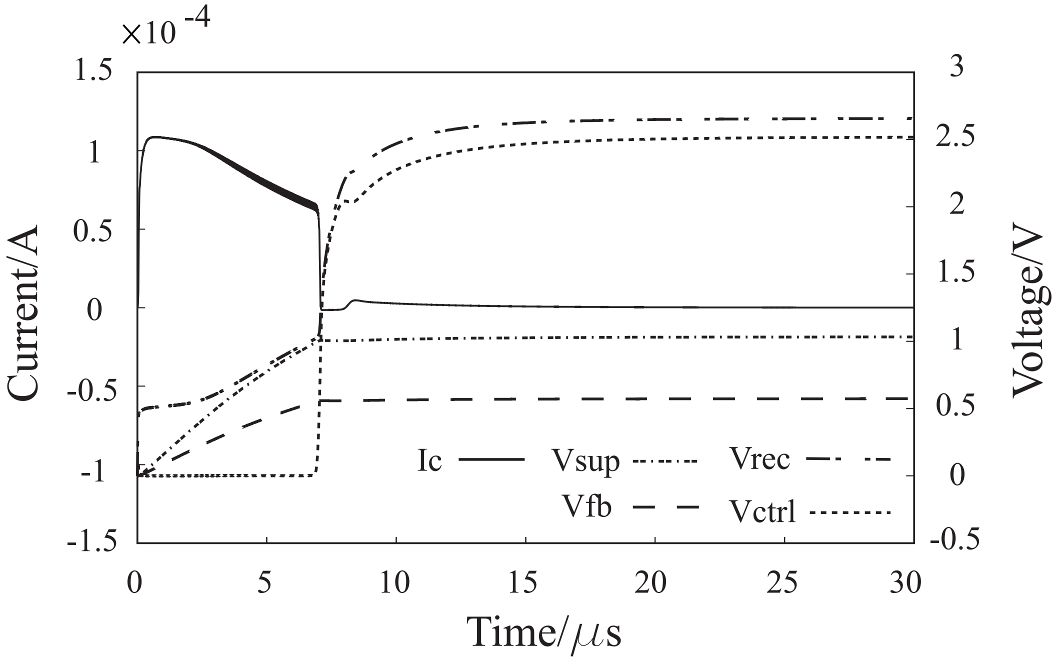


Fig. 3.8: Power-Up Phase without Power Control

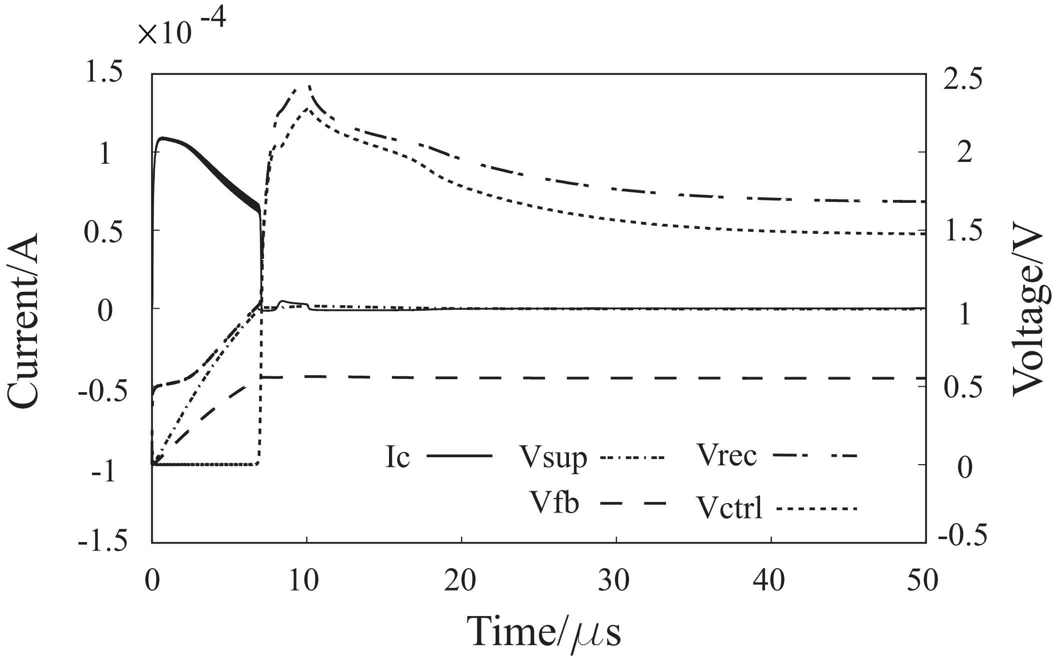


Fig. 3.9: Power-Up Phase with Power Control

quency bands have been assigned to RFID applications, such as 125KHz, 13.56MHz, 433MHz, 868MHz, $915MHz$ and 2.45GHz. Each frequency band has an individual parameter definition: modulation/demodulation, encoding/decoding etc..
ISO/IEC 18000-4 mode 1 and ISO/IEC 18000-6 type B define the same forward and return link parameters for passive transponder operating. The commands are divided into the following functional groups: selection commands, to define a subset of tags on the interrogating region; identification commands, to perform to run the multiple tag identification protocol; data transfer commands, to start the operation of reading from or writing to the tag memory [46, 47].
Mandatory operations of transponder include: delimiter checking, command decoding, CRC checking, UID or data comparison, read/write memory, CRC code generating, frame building etc.. For different commands tag performs different operations with different time cost. For example, with the 'Initialize' command, the tag shall go to the initial state without implementing comparison or memory access; with the 'Selection' command, the tag shall compare the received UID with its own UID, and then decide the further operation. In this work, the digital section of passive RFID transponders is designed and is synthesized with low-leakage standard cells from the Faraday library based on UMC 0.13-μm technology. The design contains the following functional blocks:

- Delimiter Check: check the start of the frame;
- CRC Checking: check the received frame with CRC-16;
- Serial to Parallel converter: converts the received serial data to parallel, and store the command, address, data etc to corresponding buffers;
- Command Decoder: decode the command, and give instructions to FSM;
- FSM: finite state machine, contains ready, ID, data exchange states;
- Comparator: compare the received data with the data in specific memory address;
- Collision Arbitration: includes an internal counter and pseudo random bit generator;
- Memory: synthesized with register arrays;
- Transmitter: includes CRC generating CRC-16 for the data to be transmitted; output register to store the output data.

The total area of the designed circuit is 89195μm^2.

3.4.2.2 Power Consumption of the Digital Core

In this design, the power consumption of individual functional blocks and the variation of the total power consumption over time are examined. With different commands, the tag

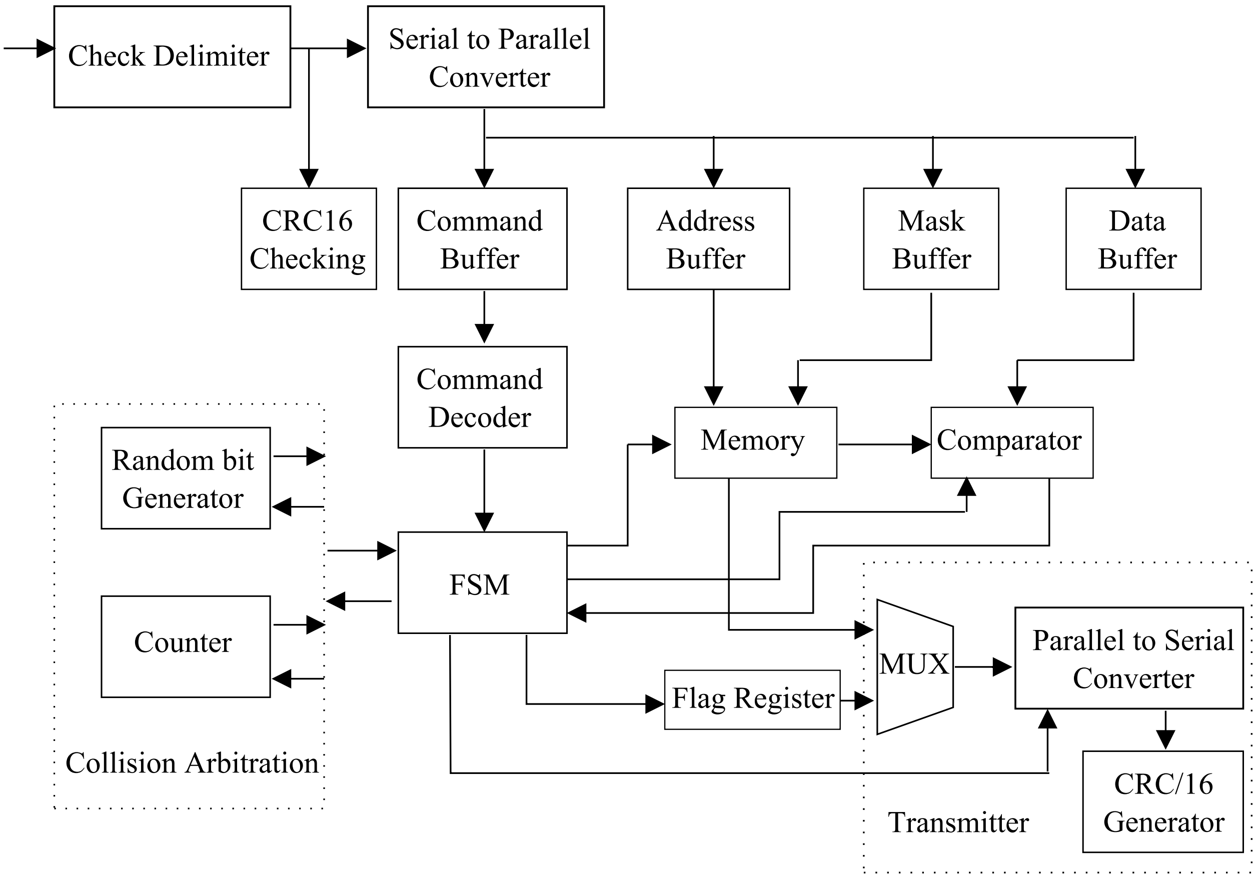


Fig. 3.10: Block Diagram of Digital Section of Transponder

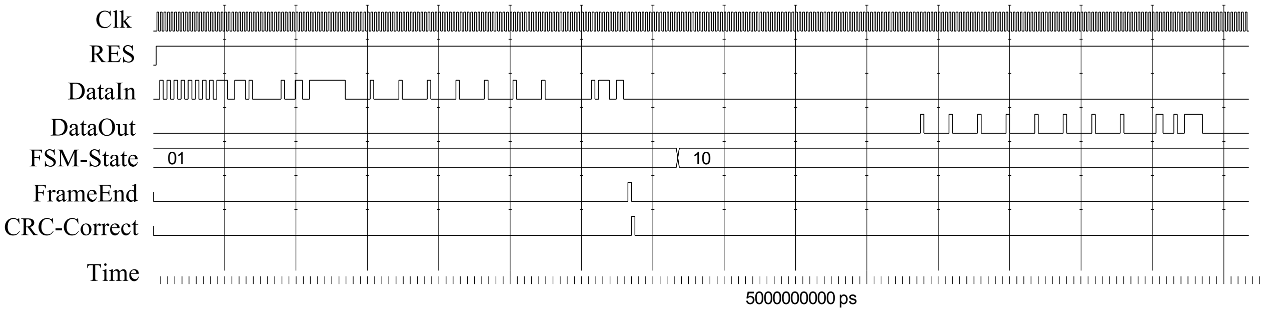


Fig. 3.11: Waveform of Tag Simulation

has different operation time and different activate function blocks. The dynamic power management strategy–clock gating technique is utilized, and the low-leakage standard cells for static power saving are employed.

For CMOS designs, the total power consumed by a circuit can be divided into two categories: static power and dynamic power. Static power is due to the reverse-biased diode leakage or source-to-drain subthreshold leakage current when the transistors are not switching. The static power is also called leakage power and is dependent on the voltage, temperature, state of transistors. The leakage power is relatively constant and independent on the logic transitions. Dynamic power is the power consumed during the logic transition. Dynamic power contains two parts: one is from the charge or discharge the load capacitors during the voltage change, and the other is the short-time short circuit current between NMOS and PMOS. The value of dynamic power consumption is strongly dependent on the switching activities [9]. The mathematical expression of total power consumption is as follows:

$$P = \underbrace{V \times I_{leak}}_{P_{leak}} + \underbrace{\langle C \times V^2 \times f + V \times I_{sc} \rangle \times N}_{P_{dyn}} \tag{3.2}$$

where, I_{leak} is the average leakage current; I_{sc} is the mean short circuit current between NMOS and PMOS and is proportional to the operating frequency; P_{leak} and P_{dyn} are the leakage and dynamic power consumption respectively; V is the supply voltage; C is the average load capacitor; N is the number of switching activities.

For passive RFID tags, the transmission data rate is around 40bit/s, and the main operating frequency of designed digital section is set as 40kHz. With this operating frequency, the switching activities are not dense, hence a low dynamic power consumption. To bring down the static power consumption, the low leakage standard cells are used. To reduce the dynamic power consumption, clock gating technique is applied, and the clock signal of those unused blocks is switched off.

3.4.2.3 Power Consumption of Individual Blocks

A test bench has been designed: the input frame with the 'Selection' command. The simulation ran for 7ms, with which the UID of the designed transponder is sent back. The tag first does the CRC checking with the received frame. Once the CRC checking is successful, the tag executes serial to parallel conversion and stores the serial data to corresponding buffers. The command decoder decodes the data in the command buffer and sends an instruction to the finite state machine. The finite state machine enables the comparator to compare the received data with the data in the received memory address. When the data received matches with that of the targeted memory address, the tag sends its UID back. Tab.3.4 shows the data of the power consumption for different function blocks. With the employment of low-leakage standard cells, the leakage power is less than 3% of the total power consumption, which is independent of switching activities and is constant over time. The dynamic power is dominant in total power consumption, which is proportional to the operation frequency and switch activities.

From Tab.3.4, it can be seen that more than 60% is consumed by memory, comparator and transmitter. These blocks are designed with an enable signal and with automatic clock gating technique from Synopsys PrimeTime, the clock gates are automatically inserted by replacing the register enable signals with gated clocks, which greatly reduced the power consumption by the clock buffer tree and hence the total power consumption.

Tab. 3.4: Power Consumption of Individual Blocks

Hierarchy	Dynamic Power/W	Leak Power/W	Total Power/W	Percentage
Digital Core	**3.954e-7**	**1.04e-8**	**4.06e-7**	**100**
Delimiter Check	1.034e-8	6.68e-11	1.04e-8	2.6
S/P converter	6.01e-8	6.72e-10	6.08e-8	15
CRC checking	2.197e-8	9.96e-11	2.21e-8	5.4
Command Decoder	1.18e-8	1.97e-10	1.20e-8	3
Comparator	9.08e-8	2.34e-9	9.31e-8	22.9
Collision Arbitration	3.55e-8	1.43e-10	3.56e-8	8.8
Memory	7.91e-8	6.15e-9	8.53e-8	21
Transmitter	7.79e-8	7.02e-10	7.85e-8	19.4
FSM	2.19e-9	2.22e-11	2.22e-9	0.5
Flag Register	5.7e-9	1.85e-11	5.72e-9	1.4

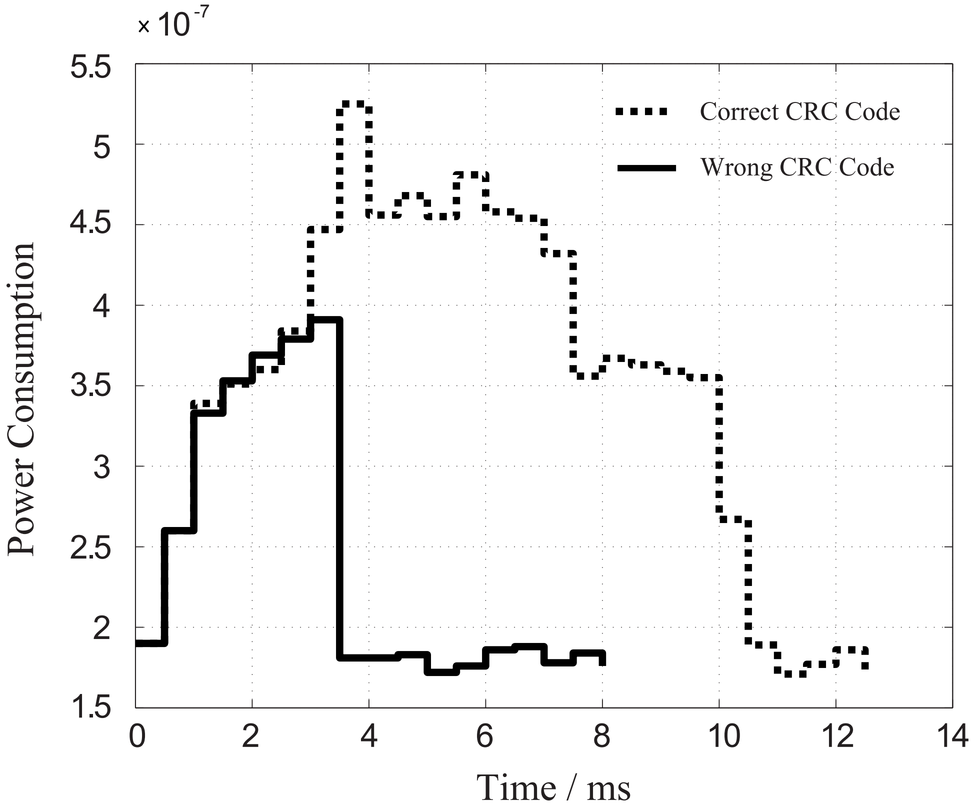


Fig. 3.12: Power Consumption Variation over time

3.4.2.4 Power consumption Variation in time domain

Two simulations are done to investigate the power consumption variation over time: one input frame with 'Selection' command, address, data and correct CRC code; the other input frame with wrong CRC code. With a wrong CRC code, the further operations like

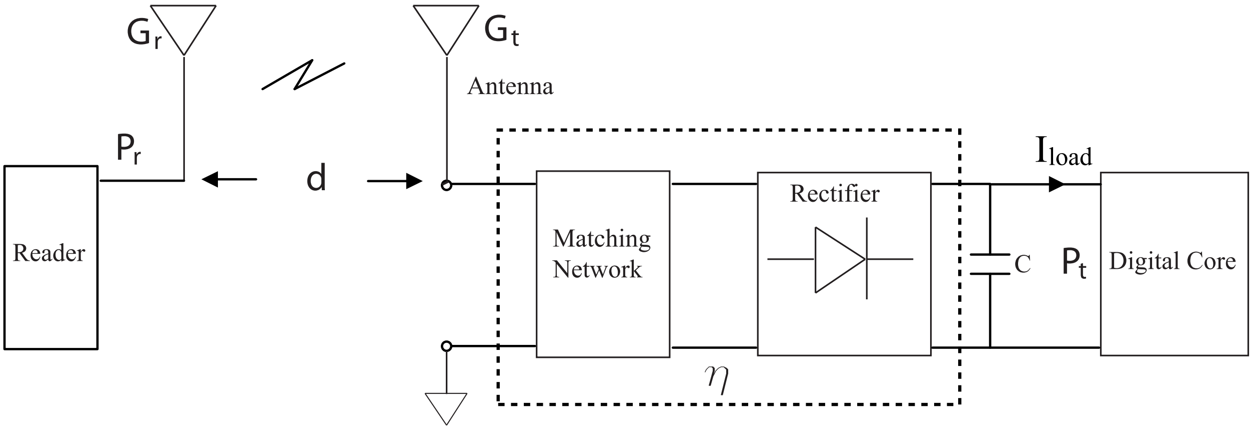


Fig. 3.13: Power Transmission Link

comparison, memory access, CRC generating are not executed. The simulations are run with a step of 0.5ms, and the power consumed by the tag is recorded. Fig.3.12 shows the power analysis over time. The solid line presents the power consumption of the tag when the CRC checking of the received frame is not correct, while the dashed line presents the power consumption when CRC checking is correct. It can be seen that the power consumption of the tag strongly varies over time. The minimum power consumption is around 0.18μW while the maximum is 0.52μW.

3.4.3 Power Transmission Link

The matching network is designed for the maximum power consumption. With less power consumption, mismatch happens, and the power transmission still ensure the power requirement at the tag. However, the power conversion efficiency is strongly reduced. Take the 'Selection' command with correct CRC checking as an example. Assuming that the overall power conversion efficiency (including the power transfer efficiency of the matching network) is 30% [139], with maximum power consumption of 0.52μW, the received power of the antenna has to be at least 1.73μW in order to obtain the maximum load current. When the transponder operates consuming less power, for example, 0.18μW, the power utilization efficiency is only 10%. In this case, if a matching network is tuned with a feedback control signal, and a reader with automatically adaptive emitted power, a considerable portion of power will be saved.

Fig.3.13 shows the power transmission link between reader and tag. The power emitted from the reader is P_r; the reader antenna gain is G_r; the transmission distance is d; the tag antenna gain is G_t; overall power conversion efficiency including the power transfer efficiency of the matching network and the power conversion efficiency of the power harvesting network is η; the power consumption of the tag is P_t, and the operation frequency is f_c. The power transmission link can be expressed with the following equation:

$$P_t = \quad P_r + 147.6 - 20log(d) - 20log(f_c) + 10log(G_r) + 10log(G_t) + 10log(\eta) \tag{3.3}$$

For simplicity, it is assumed that an omnidirectional antenna for both reader and tag is employed, and the antenna gain is 1. The distance is set as 10m, and the operation frequency is set as 2.45GHz for calculation. The optimal overall power conversion efficiency is set as 30%. Without employing the adaptive power emission at the reader and automatic matching network at tag, the power emitted from reader has to fulfill the maximum power consumption of the transponder. With the above assumptions, maximum value of P_t equals 0.52μW, which results a P_r = 1.8W. To execute the 'Selection' command, the average power emission is 1.8W. With employing the adaptive power emission at the reader and the automatic matching network at tag, the power transfer efficiency of the matching network is supposed to be optimised for all load power consumptions. The reader emits power adaptively according to the tag's needs, with the maximum emitted power 1.8W, and minimum emitted power 0.625W. To execute the 'Selection' command, the average power emission is 1.2W, which saves 33% emission power.

3.5 Automatic Power Control

Based on the theoretical analysis in the previous section, it is necessary to build a reader with the ability of controlling the emission power according to the power consumption of transponders. Besides, for a cognitive reader which can communicate with tags designed based on different protocols, the power emission has to be tuned in real-time, but differently for varying tags.

The following two aspects are considered: first, the control of power emission of the reader has to be adjusted for different protocols; second, the effect of the power emission controlling on data demodulation at the transponder.

3.5.1 Dependency on Protocols

There are many distinct protocols [26, 46, 47] for RFID systems. Each protocol has different specifications for the design of transponders: forward and return link parameters (Manchester/PIE data encoding, 64-bit/96-bit EPCs (Electronic Product Code)), anticollision algorithms (ALOHA, Binary Tree), error detection (16-CRC, 5-CRC), command sets, etc..

The difference in design specifications results in different designs of transponders, and hence different power consumption variations over time. Therefore at the reader side, the power emission has to be controlled in real-time for different commands and differently for various protocols. In this work, for demonstration purpose, the digital section of two passive transponders in compliance with ISO 18000-4/6 is designed, with the

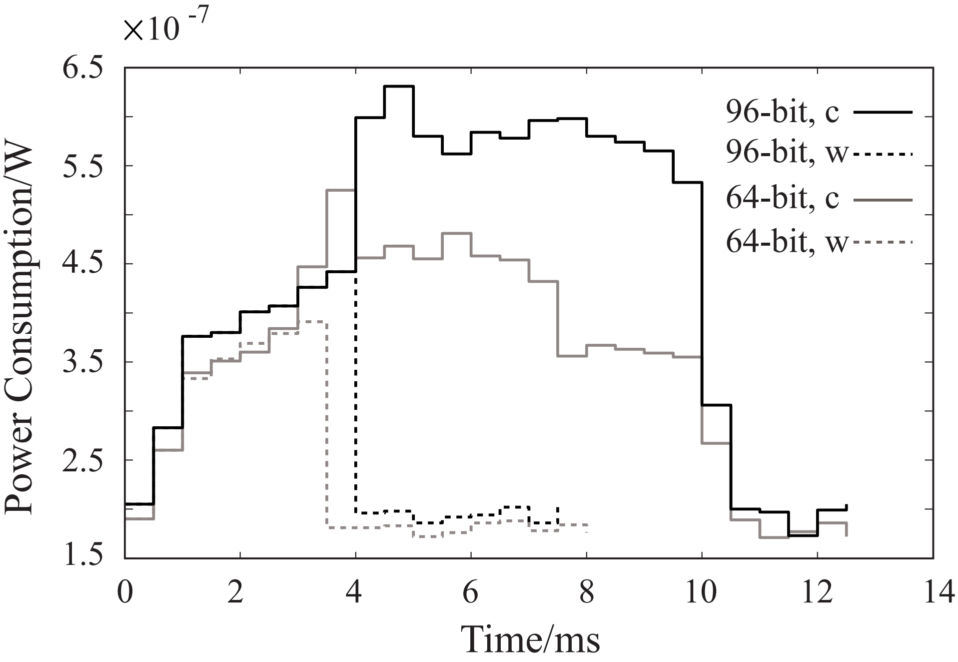


Fig. 3.14: Power Consumption Variation for 64-bit/96-bit EPCs. ’96-bit, c’: correct CRC with 96-bit EPC; ’96-bit, w’: wrong CRC with 96-bit EPC; ’64-bit, c’: correct CRC with 64-bit EPC; ’64-bit, w’: wrong CRC with 64-bit EPC;

length of EPC for 64-bit and 96-bit respectively. The power consumed by the transponders is evaluated with Synopsys PrimeTime. The test bench with a ’selection’ command with correct and wrong CRC coding is applied for both designs. The simulation result is shown in Fig.3.14. It can be seen that the power consumption envelope of the transponders differs due to the difference in the length of EPC. Therefore, in order to utilize the power effectively, the reader needs to control the power emission differently according to the regulations. If an automatic tuneable matching network before the power harvesting circuit is employed in transponders which enables a relatively constant conversion efficiency from reader’s emission and rectifier’s DC output [139], and instead of emitting a constant power level, an adjustable reader emits power with an amplitude envelope according to the power consumption variation of transponders, the theoretical evaluation showed that the reader could save as much as 33% power for 64-bit EPC and 31.8% for 96-bit EPC.

3.5.2 Dependency on Modulation Schemes

The common modulation types are: FSK, PSK, ASK. Both FSK and PSK signals have constant envelope, with which the RF power can be transmitted continuously even during the data transmission. However, those two modulation schemes are not recommended for forward (from reader to transponder) data transmission, since the hardware requirement, such as mixer, oscillator etc., is very high for passive transponder design. ASK is the

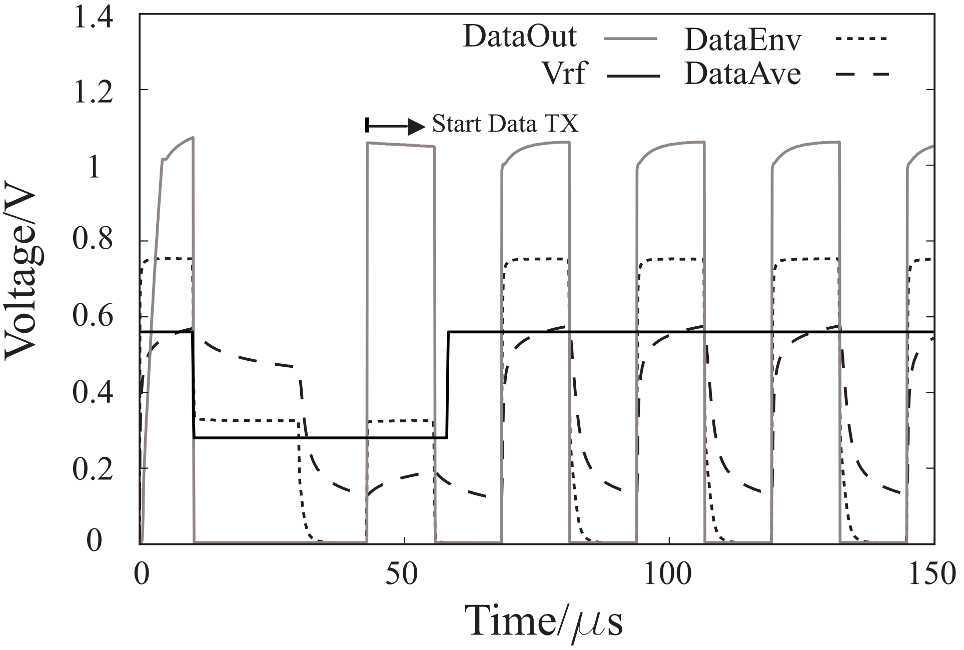


Fig. 3.15: Data Demodulation with Power Control. 'DataOut': demodulated data; 'Vrf': the voltage level of RF signal; 'DataEnv': the detected envelope; 'DataAve': the average signal.

most common modulation scheme in prevalent protocols, for the demodulation is easy to be implemented in passive transponders. In this work, the ASK modulation has been considered. The effect of power modulation on forward data transmission is analyzed. The rate of power control must be defined such that the bit-error-rate at the transponder is not increased. In RFID transponder, ASK-modulated data can be recovered by comparing the envelope with the average signal. The principle is to use an envelope detector to obtain the envelope, and then use a RC network with large time constant to achieve the average level [14]. A hysteretic comparator compares the envelope and the average signal and decides the output data. When the power control is involved, the amplitude of received RF signal is not only modulated according to the input data but also changed due to the control of power emission. Fig.3.15 depicts the detected envelope of the received RF signal before and after activation of the power control. At the beginning of the simulation, only continuous RF signal is sent for power-up; after the power-up phase is done, the RF signal level is reduced; then the data transmission starts, and later the RF signal level is increased.

To examine the effect of the power control on data transmission, the simulation is performed with the model built in Matlab Simulink, please refer to Fig.3.5. The input signal of the power amplifier at the reader transmitter can be expressed as:

$$S(t) = [\sum_{k} x_k g(t - kT_s)] cos(\omega_c t) \tag{3.4}$$

where, $x_k \in [0, 1]$ is k-bit data of I-channel, for double-side band 100% ASK modulation, Q-channel has no data; T_s is the bit period; ω_c is the carrier angular frequency, and $g(t)$ is the impulse response of raised cosine filter. In current modelling, the bit period is $12.5\mu s$, and carrier frequency is 2.45GHz. And the signal at the output of the power amplifier with variable gain is:

$$S_{PA}(t) = G_{PA} * S(t) * \sum_{m} (1 - A_m) * r(t - mT_p); \tag{3.5}$$

where, T_p is the power control rate; A_m is the power control depth; $r(t)$ is rectangular function; G_{PA} is gain of power amplifier. The output signal of power amplifier is sent over the reader antenna, wireless channel and tag antenna before it comes to envelope detector and average circuit. For current analysis, the nonlinear effect of the antennas and the noise of the wireless channel are neglected. The envelope signal can be written as:

$$\begin{aligned} S_{EN}(t) = \; & G_{AC} * G_{PA} * [\textstyle\sum_k x_k g(t - kT_s)] \\ & *[\textstyle\sum_m (1 - A_m) * r(t - mT_p)] \end{aligned} \tag{3.6}$$

where, G_{AC} is the combined gain of the antenna and channel. The average signal can be written as:

$$\begin{aligned} S_{AVR}(t) = \; & \tfrac{G_{AC} * G_{PA}}{nT_s} * \textstyle\int_{t-nT_s}^{t} \{[\sum_k x_k g(t - kT_s)] \\ & *[\textstyle\sum_m (1 - A_m) * r(t - mT_p)]\} dt \end{aligned} \tag{3.7}$$

where, nT_s represents the average time constant. Fig.3.16 shows two plots: in the first simulation, the power control rate is set as 0.5ms, which is 40 times of the bit period, and the time constant of average circuit is varied from $2T_s$ to $20T_s$; in the second one, the time constant of average circuit is fixed with $4T_s$, and the power control rate is varies from 0.1ms to 1ms. The bit-error-rate is examined for both cases. The result shows the larger the time constant of the average circuit or the faster the power control rate, the higher the bit-error-rate. To ensure that the power control does not affect the data demodulation, the time constant of the average circuit must be much smaller than the power control rate so that the average level can follow the change of the power level. From the other side, the time constant of average circuit must be designed much larger than that of envelope detector, in order to achieve the average level of received signal and also depress the noise through average operation.

3.6 Summary

In this part, the power consumption of passive RFID transponders is analyzed. The analysis considers both power-up and communication phases. Based on the analysis, a new architecture for RFID reader was proposed. The concept of automatic power control with the possible realization with SDR techniques is presented. Till now, only the situation of one reader with only one transponder in interrogation region is considered. The perspective for future work is to find a solution for saving power in power-up phase when

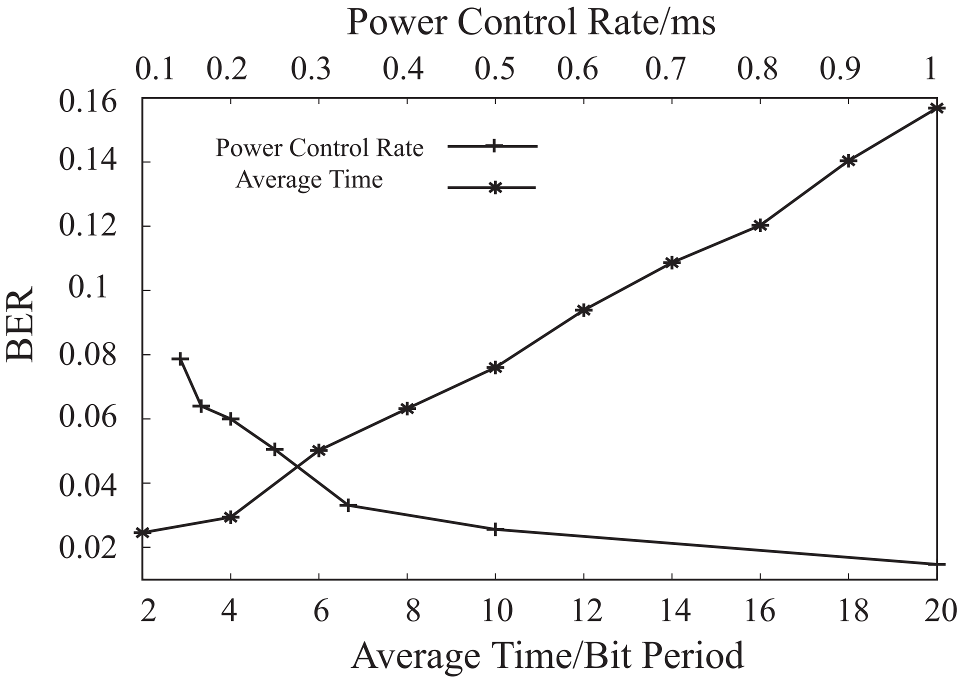


Fig. 3.16: Bit-Error-Rate Over Average Time Constant and Power Control Rate.

multiple transponders exist in the interrogation region. The digital section of the passive transponder is designed in compliance with ISO/IEC 18000-4/6. The power consumption of the transponder is estimated under different operations, considering both static and dynamic power consumption. The real-time operation-dependent analysis of the power consumption is then done, and the simulation result is analyzed, with the suggestion of employing a tuneable matching network in order to maximize the overall power conversion efficiency. The achieved result can be used to aid the design of a feedback controller for automatic impedance matching. A novel multi-protocol RFID reader with automatic power control is proposed in this paper based on a software defined radio architecture. The transponder power consumption variation over time is considered for different protocols. The modulation effect of power control on forward data transmission is included in the analysis. The emission power of the reader is automatically tuned in real-time according to the needs of the transponders in compliance with different standards, with which a considerable amount of power can be saved.

Chapter 4

Characterization, Modelling and Design of a RF Energy Harvester

Contents

Batteryless portable devices like wireless sensor node harvest energy from different sources: RF (ambient or actively directed UHF/HF), vibrational (piezo, electromagnetic etc.), photovoltaic and thermal [120]. For each approach, different energy transduction mechanisms are established. AdaptivEnergy summarized and divided typical power harvesting solutions into four main building blocks: energy harvester, conversion electronics, energy storage and energy delivery [1]. The conversion electronics play a significant role in the energy usage efficiency. Classified methodologies directed towards different transducers have been developed for improving the power conversion efficiency: active energy extraction circuitry for vibrational energy harvester [53]; maximum power point tracking for photovoltaic [11] and thermal energy harvesters. Many investigations have also been dedicated to designing RF energy harvesters, of which most applications targeted passive RFID tags and wireless sensor nodes.

Based on the system-level analysis in the former chapter, the reader shall emit the power according to the need of the transponder to save the power consumption. In the transponder, a RF-DC power harvester is normally employed to collect the power for supplying the operation. As seen from the designed transponder, the power consumption is not constant but variant over time. To harvest the power distributed according to needs, the power harvesting circuit shall be adjusted according to the change of the power consumption of the transponder.

State-of-the-art design [17, 119], however, devote less investigation to the effect of the dynamic power consumption of the transponder on the overall power conversion efficiency. In this work, a methodology to analyse the power harvesting circuit with the focus on the effect of dynamic load current consumptions on the input impedance is proposed. The analysis showed that the overall power conversion efficiency was dramatically decreased at different current load with mismatching, e.g. from 30.1% to 2.3% as the load current changes from $1\mu A$ to $10\mu A$. The result suggests the necessity of dynamically optimising the impedance matching network between the antenna and the rectifier according to the transponder operation status.

In this chapter, the analysis of the RF-DC power harvester with dynamic loads has been focused and a new approach is investigated by adjusting the RF matching network according to the operation conditions with the aid of a feedback control. In chapter 4.1, the performance index of designing a RF energy harvester is reviewed. After that, in chapter 4.2, with the objective to simplify the analysis, a compact I/V model of diode-connected transistors working in strong-inversion and subthreshold is developed. Based on the model, in chapter 4.3 the voltage sensitivity of the circuit is derived and analyzed. A load-dependent large-signal input resistance model and the minimum power required to achieve a certain DC voltage supply with variable load currents are then derived. Then in chapter 4.4 the concept of an operation-controlled tuneable matching network is proposed in order to maximize the overall power efficiency. Then a prototype design of the power harvesting circuit is presented in chapter 4.5, where the design principle and the basis of employing an auxiliary rectifier are explained; finally the results based on the post-layout simulation and measurement are presented, and the power delivery performance with the proposed harvesting circuit is compared and analysed.

Both the input impedance derivation and the prototype design in this chapter are based on a conventional charge-pump rectifier which employs diode-connected transistors of the UMC 0.13-μm technology based on the BSIM3v3 MOSFET model [113].

4.1 Performance Index of RF Energy Harvester Design

In passive far-field UHF/microwave RFID transponders, a power harvesting circuit is employed for converting part of collected RF power to DC power supply voltage. A matching network is usually applied between the antenna and the power harvesting circuit to ensure the maximum power transfer, as depicted in 4.1

The most important figures of designing a RF power harvester are power transfer efficiency, power conversion efficiency (PCE), power/voltage sensitivity. The power transfer efficiency is defined as the power transferred to the rectifier over the power received by the antenna:

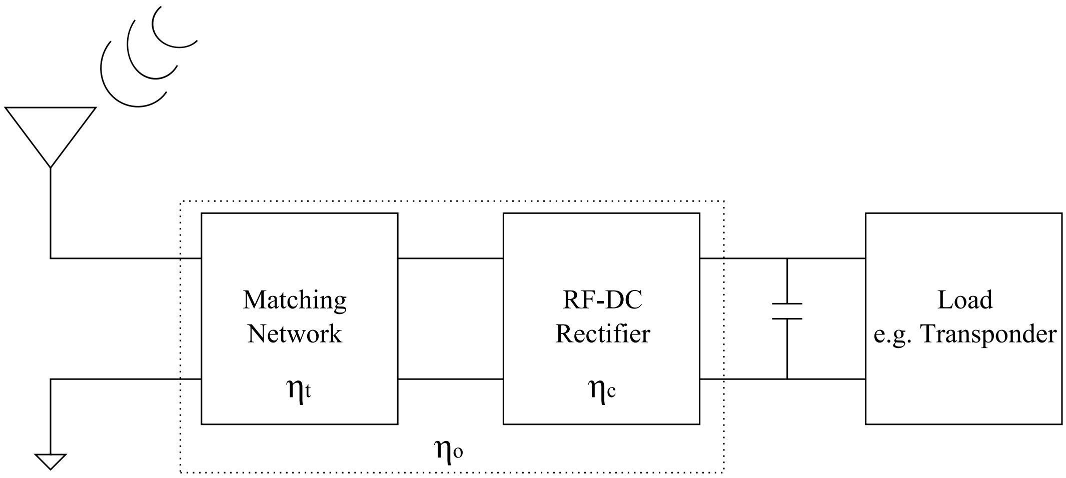


Fig. 4.1: RF-DC Energy Harvester

$$\eta_t = \frac{P_{in} - P_{re}}{P_{in}} \tag{4.1}$$

where, P_{in} is the incident RF power at the antenna, and P_{re} is the reflected RF power due to the impedance mismatch. Power conversion efficiency is a key parameter of the rectifier, which is defined as the output DC power P_{DC} over the RF power at the input of the rectifier [17]:

$$\eta_c = \frac{P_{DC}}{P_{in} - P_{re}} \tag{4.2}$$

And the overall efficiency of the energy harvester is defined as:

$$\eta_o = \frac{P_{DC}}{P_{in}} \tag{4.3}$$

Many efforts have been devoted to the optimization of the RF-DC rectifiers by finding the optimum design topologies and design parameters, e.g. the number of stages and size of the transistors used in the circuit, aiming to maximize the power conversion efficiency. Yi et al. [126] developed an analytical model for the charge-pump rectifier built of MOS transistors, and based on the model the optimal transistor size and stage number can be derived to maximize the power conversion efficiency of the rectifier. Mazzilli et al. [76]

and Zhu et al. [134] compared different rectifier structures with the aspect of power conversion efficiency and voltage conversion efficiency, individually, and presented criteria to choose the appropriate rectifier topology according to the design requirement.

Power/voltage sensitivity is the minimum input power/voltage level, which is required at the input of the rectifier, to achieve a certain output dc voltage with a given load current [102]. To maximize the power/voltage sensitivity is essential of improving the communication distance. Shameli et al. [102] proposed a method of improving the rectifier sensitivity by using voltage boosting technique, in which the high ratio between the impedance values at the input port of the rectifier and the antenna is utilized, with the premise of optimal power transfer.

To improve the power transfer efficiency, an impedance transformation network is employed to match the antenna source impedance to the input impedance of the rectifier, which is usually modelled as a parallel R-C network. Most of state-of-the-art design have assumed the input impedance of the rectifier a constant value [72] or relatively steady value [119], and the matching network is correspondingly designed as a fixed one. In case that the load consumption is not constant, the matching network was suggested being designed by matching with the maximum current consumption [17], indicating the worse power sensitivity and less overall power conversion efficiency.

The effect of the impedance variation due to the dynamic consumption of current on the power transfer is not yet well investigated in RF power harvester design. In passive transponders, the load circuit of the rectifier has several different operations, i.e. compare, read/write, idle [47], and the consumed current varies for each operation, as noted in Chapter 3.4. The impedance, seen from the input of the power harvesting circuit, varies with the change of the consumption current of the transponder. Therefore, an optimal matching network for one operation cannot realize maximum power transfer for other operations. To improve the power transfer efficiency by matching the rectifier to the antenna, many factors must be taken into account, i.e. incident power density P_{in}, load condition I_{Load}, nonlinear effect of the voltage rectifiers, design technology, etc.. Due to the non-linear effect, the input impedance of the voltage rectifier is not constant but depends on both the incident RF power level and the output load:

$$Z_{in} = f(P_{in}, I_{Load}) \tag{4.4}$$

To design a matching network for maximum power transfer, a deeper investigation of the rectifier input impedance must be done. Barnett et al. [7] [6] developed a mathematical expression for the input impedance of the rectifier built of schottky diode as a function of the load current consumption. To guarantee the impedance match between antenna and voltage rectifier over diverse operation conditions, different techniques are explored. In [21] and [81]'s work, to maximize the power delivery over a wide range of incident power density, a DC matching technique was proposed with periodically tuning the emulated the resistance load of the rectenna by using a boost converter, referred as MPPT technique, which has been well employed in other harvesting techniques [11].

4.2 Analysis of Power Harvesting Circuit

A power recovery circuit is shown in Fig.4.2, which consists of the antenna model, L-match impedance transformer and an N-stage doubler. Multi-stage doublers have been widely used for power recovery circuit design [7, 52, 57, 102, 114]. By using the cascaded doubler, the DC output voltage can be raised to a high value with small incident RF power. Each stage uses the DC voltage output of the preceding stage as a base voltage, in such a way, the DC voltage of each stage is accumulated. (Single stage doubler works in positive and negative phase, how the current flows, illustration of rectification mechanism) The DC voltage output of an N-stage doubler is:

$$V_{DC} \approx 2N * (V_{RF} - V_{th}) \tag{4.5}$$

where, V_{RF} is the amplitude of the incident RF signal; V_{th} is the threshold voltage of the MOSFET/diodes; N is the stage number. Curty et al. [17] proposed a classical model for micro-power rectifiers, and defined the steady working state for the rectifier in which the current through each transistor is steady. In this work, the same criteria have been followed: the charging process where the output voltage is not yet constant is ignored and once the output voltage and the current flow through the transistors get steady, the rectifier operates is considered in a steady state.

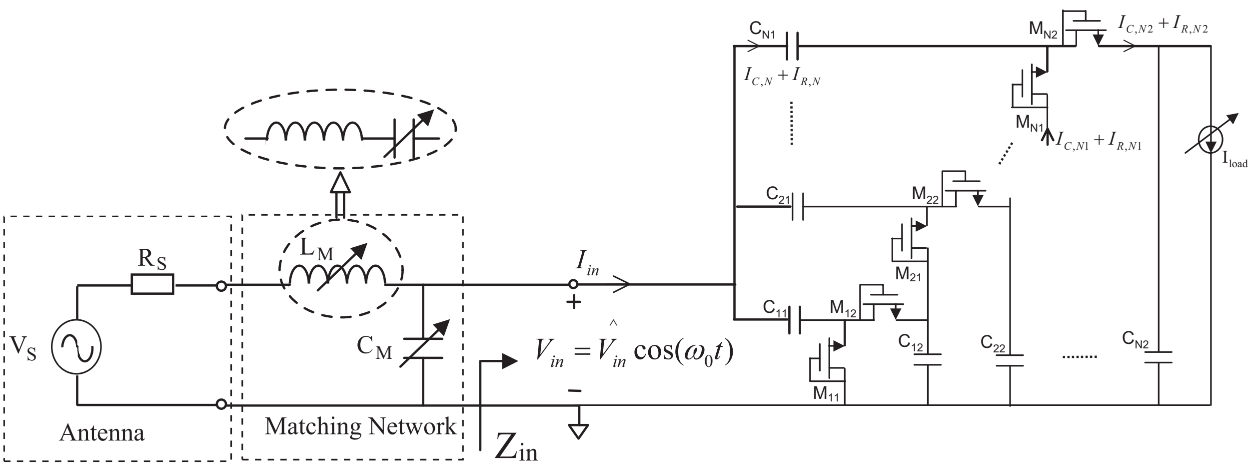


Fig. 4.2: Power recovery circuit

Fig.4.3 gives the input current of the N-th doubler, and the current is constructed by two parts: the 90^0-phase-shifted part $I_{C,N}$, which is due to the parasitic capacitance of the transistors, and the in-phase part $I_{R,N}$, which is from the DC response of the transistors. By using the same transistor and charge-pump capacitors, the input current of the N-stage rectifier is:

$$I_{in} = \sum_{i=1}^{N} I_{C,i} + I_{R,i} \approx N \cdot (I_{C,N} + I_{R,N}) \tag{4.6}$$

The input impedance is then calculated as:

$$Z_{in} = \frac{V_{in}}{N \cdot (I_{C,N} + I_{R,N})} = \frac{1}{N \cdot j\omega_0 C_{in,N} + \frac{N}{R_{in,N}}} \tag{4.7}$$

The input impedance is modelled as the parallel connection of a resistance $R_{in,N}/N$ and a capacitance $N \cdot C_{in,N}$, where $C_{in,N}$ and $R_{in,N}$ are the input capacitance and resistance of the N-th doubler. The in-phase current of the N-th doubler $I_{R,N}$ is the summation of the drain-source currents $I_{R,N1}$, $I_{R,N2}$ of M_{N1} and M_{N2}. When M_{N2} is forward biased, M_{N1} is reverse biased, therefore, $I_{R,N1}$ has a half period time shift and an opposite direction, as shown in Fig.4.3. For a charge-conservative transistor, the integration of $I_{C,N2}$ over one period is 0, therefore, the charge through the transistor M_{N2} which is denoted as ΔQ_{MN2} and the charge consumed by the load ΔQ_{Load} can be expressed as:

$$\begin{aligned} \Delta Q_{MN2} &= \int_{t_0}^{t_0+T} I_{R,N2} dt \\ \Delta Q_{Load} &= \int_{t_0}^{t_0+T} I_{load} dt \end{aligned} \tag{4.8}$$

Due to the charge conservation law, the charge through the transistor M_{N2} is equal to the charge consumed by the load [126]:

$$\begin{gathered} \Delta Q_{MN2} = \Delta Q_{Load} \\ \int_{t_0}^{t_0+T} I_{load} dt = \int_{t_0}^{t_0+T} I_{R,N2} dt \end{gathered} \tag{4.9}$$

The change of the load current greatly affects the amplitude of $I_{R,N2}$, while the value of $I_{C,N2}$ is influenced marginally. Hence, a considerable variation of the input resistance and a stable parallel capacitance due to the change of the load current are expected.

4.2.1 Modelling Strategy

The analysis is started from the last stage of the rectifier. For a diode-connected transistor, the gate terminal is connected to the drain terminal. The transistor works in different regions of its I/V model: strong inversion (saturation), subthreshold, reverse-leakage [113], as depicted in Fig.4.5. Four different working regions of MOS transistor from the sinusoidal waveform of Vin(t) and Vo(t) in one cycle are described as [126]:

- Subthreshold region [t1,t2]: From t1, the voltage over from drain to source terminal is positive, and the gate source voltage is smaller than the threshold voltage. MOS transistor M_{N2} starts to conduct current and to work in the weak-inversion region. The charge through the transistor while working in this region is denoted as ΔQ_{sub1}.
- Superthreshold region [t2,t3]: From the time t1, the gate source voltage gets larger than the threshold voltage and M_{N2} starts working in saturation region. The charge through the transistor while working in this region is denoted as ΔQ_{super}.

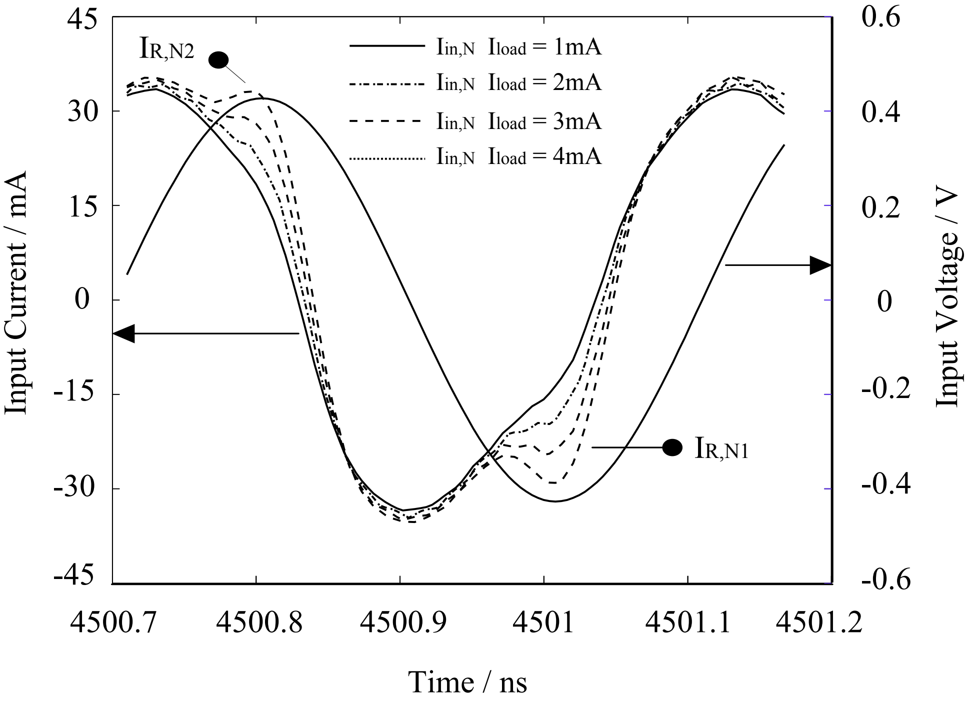


Fig. 4.3: Input current of the last stage of a 3-stage rectifier with different load currents. The transistor size W/L is 2μm/0.12μm, and input voltage amplitude is 0.427V

- Subthreshold region [t3,t4]: The difference between drain and source voltages remains larger than 0 and the gate source voltages gets smaller than the threshold voltage. Therefore, M_{N2} again enters the subthreshold region. The charge through the transistor is denoted as ΔQ_{sub2}.
- Leakage region [t4,t1+T]: From t4, the output voltage rises larger than the input voltage. Drain and source terminals of M_{N2} interchange with each other. Gate source voltage is zero which is smaller than the threshold voltage, and M_{N2} works in the subthreshold region and conducts a reverse current. The charge through the transistor while working in this region is denoted as ΔQ_{leak}.

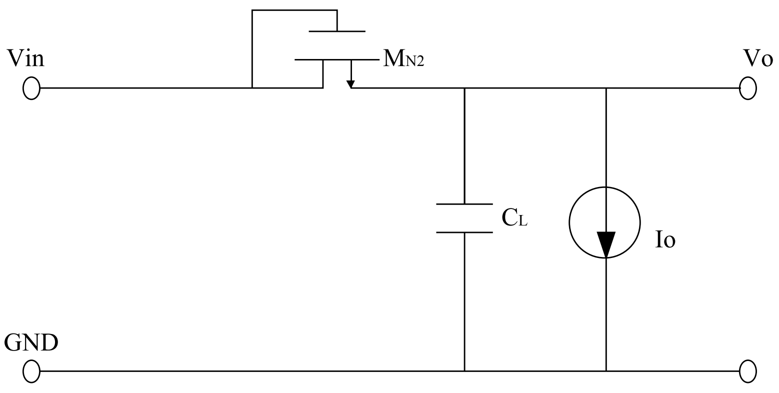


Fig. 4.4: Last-stage of the rectifier

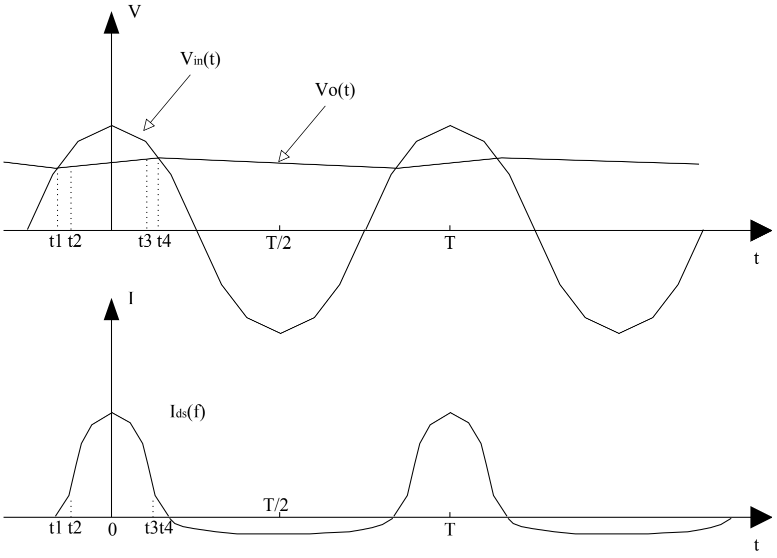


Fig. 4.5: Waveforms of Input and Output Voltage, Transistor Current [126]

Due to the charge conservation law, the current of strong inversion and subthreshold has to compensate the charge consumption of both load current and reverse leakage current.

$$\Delta Q_{MN2} = \Delta Q_{sub1} + \Delta Q_{super} + \Delta Q_{sub2} - \Delta Q_{leak} \tag{4.10}$$

With combining the current in first three forward conductive regions:

$$\Delta Q_{sub1} + \Delta Q_{super} + \Delta Q_{sub2} = \int_{t_0}^{t_0+T} I_{R,S,N2} dt \tag{4.11}$$

Eqn.(4.8) is rewritten as:

$$\Delta Q_{MN2} = \int_{t_0}^{t_0+T} I_{R,S,N2} dt - \int_{t_0}^{t_0+T} I_{R,L,N2} dt \tag{4.12}$$

And Eqn.(4.9) is then reformed as:

$$\int_{t_0}^{t_0+T} \underbrace{(I_{load} + I_{R,L,N2})}_{I_{load}^{eff}} dt = \int_{t_0}^{t_0+T} I_{R,S,N2} dt \tag{4.13}$$

where, $I_{R,S,N2}$ is the drain-source current of M_{N2} when it works in strong inversion and subthreshold region, $I_{R,L,N2}$, is the reverse leakage current of M_{N2}, and I_{load}^{eff} represents the effective load current which includes the reverse leakage current [126]. The reverse leakage current strongly depends on the transistor size, therefore, In this work, for simplification, the reverse leakage current is modelled as $I_o \cdot W$, where I_o is the time-average leakage current of unit transistor width, which can be achieved from simulation.

4.2.2 BSIM3v3.2.2 MOSFET I-V Model

To find an analytical expression for the input current as a function of the load currents based on (4.13), the transistor I/V model needs to be employed. Individual expressions have been given in BSIM3v3.2.2 for the drain current in all operating regions. In the subthreshold region, the drain current equation is expressed as:

$$I_{ds} = I_{s0}(1 - exp(-\frac{V_{ds}}{v_t}))exp(\frac{V_{gs} - V_{th} - V_{off}}{nv_t}) \tag{4.14}$$

with I_{s0}:

$$I_{s0} = \mu_0 \frac{W}{L} \sqrt{\frac{q\epsilon_{si} N_{ch}}{2\phi_s}} v_t^2 \tag{4.15}$$

In strong inversion (saturation) region, the drain current with considering substrate current induced body effect is expressed as:

$$I_{ds} = Wv_{sat}C_{ox}(V_{gs} - V_{th} - A_{bulk}V_{dsat})(1 - \frac{V_{ds} - V_{dsat}}{V_A})(1 + \frac{V_{ds} - V_{dsat}}{V_{ASCBE}}) \tag{4.16}$$

Part of the parameters in BSIM3v3.2.2 for MOSFET are listed in Tab.4.1

Besides, in BSIM3v3, a single unified function is also given to express the transistor drain current in all operation regions. However, a large number of parameters as well as complex equations limit its application in building analytical models. Instead of using the

Tab. 4.1: Parameters Used in BSIM3v3.2.2

Abbr.	Description
μ_0	Electron mobility
q	Electron charge
ϵ_{si}	Silicon permittivity
N_{ch}	Doping concentration in the channel
v_t	Thermal voltage
ϕ_s	Surface potential
V_{th}	Threshold voltage
V_{off}	Subthreshold region offset voltage
W	Transistor width
L	Transistor length
n	Subthreshold region swing parameter
C_{ox}	Gate capacitance per unit area
A_{bulk}	Bulk charge effect parameter
V_A	Early voltage
V_{ASCBE}	Early voltage due to substrate current induced body effect
v_{sat}	Saturated carrier drift velocity
V_{dsat}	Saturation voltage

BSIM transistor model, a compact model is proposed for transistors working in strong inversion and subthreshold region. For further simplification, the reverse leakage current is considered by evaluating the average value over a period.

4.2.3 Compact I/V Model of Transistor

The transponder requires a certain supply voltage range in order to ensure the steady power supply for both analog and digital section. In order to increase the supply current, the source voltage of M_{N2}, which is equal to V_{out}, has to be brought down so that the drain-source current of M_{N2} is increased to fulfill the charge consumption of the load. Therefore, the supply voltage range also limits the current supply capability of the rectifier. The transistors of the rectifier work in a restricted voltage environment. With this limitation, the compact I/V model for strong inversion and subthreshold region is developed as following:

$$I_{R,S,N2} = a \cdot \frac{W}{W_0} \cdot e^{x-y\cdot V_{out}} \cdot e^{b\cdot V_{ds,N2}} \tag{4.17}$$

with the drain-source voltage of M_{N2} $V_{ds,N2}$ as:

$$V_{ds,N2} = V_{in} + V_{b,N1} \approx V_{in} - \frac{1}{2N} \cdot V_{out} \tag{4.18}$$

where, W_0 is 1μm; V_{out} is the output voltage; $V_{b,N1}$ is the boosting voltage of charge-pump capacitor C_{N1} [126]; N is the stage number of the doublers; a,b,x,y are four parameters achieved with curve fitting. The proposed I/V model is verified by comparing with simulation results based on BSIM3v3. The load current is varied from $1\mu A$ to $10\mu A$, and the DC output voltage is $0.5V$. The time-domain simulation is implemented in SPICE, and the current is plotted and shown in Fig.4.6.

Tab. 4.2: Parameters for Curve Fitting

Variable	a	b	x	y
Value	0.11e-7	24.85	0.75	-0.3

By evaluating the average reverse leakage current, and considering the load current constant over a period, Eqn.(4.17) can be written as:

$$I_{load}^{eff} \cdot T = \int_{t_0}^{t_0+T} a \cdot \frac{W}{W_0} \cdot e^{x-y\cdot V_{out}} \cdot e^{b\cdot(V_{in}-\frac{V_{out}}{2N})} dt \tag{4.19}$$

and the relation between the output voltage and the load current as well as the input voltage is expressed as:

$$V_{out} = \frac{1}{-y-2b} \cdot ln(\frac{I_{load}^{eff} \cdot T}{a \cdot \frac{W}{W_0} \cdot e^{x} \cdot \int_{t_0}^{t_0+T} e^{b\cdot\widehat{V}_{in}cos(\omega_0 t)} dt}) \tag{4.20}$$

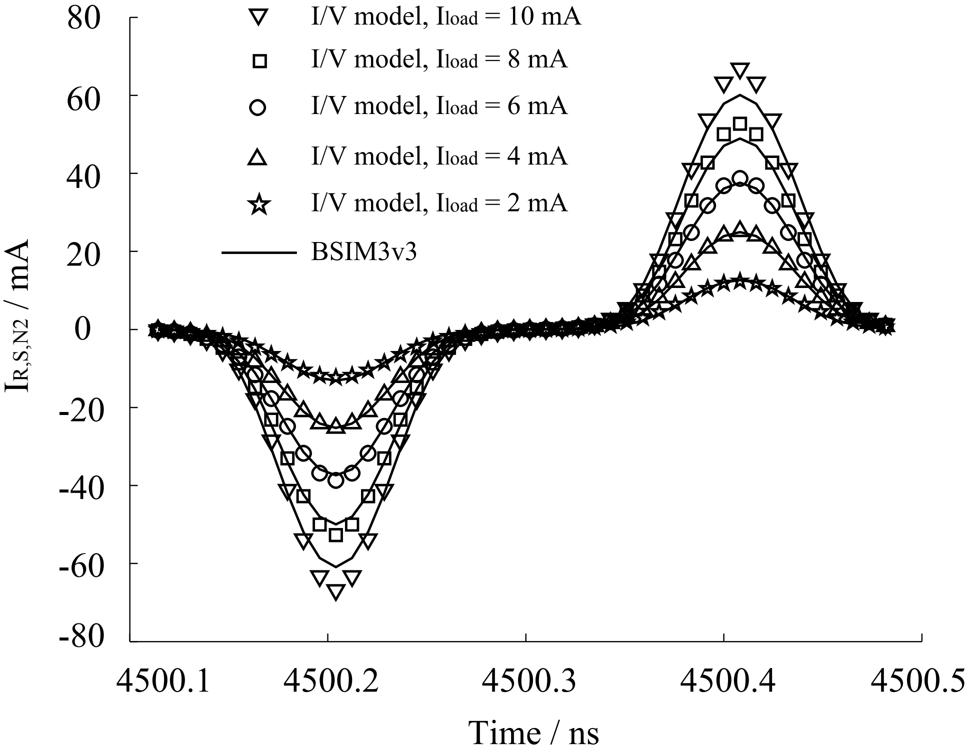


Fig. 4.6: Drain-source current of M_{N2} with different load currents in strong inversion and subthreshold regions. Number of stages is 3, and transistor size W/L is 2μm/0.12μm.

By substituting (8) to (5), the drain-source current $I_{R,S,N2}$ is expressed as:

$$I_{R,S,N2} = \frac{I_{load}^{eff} \cdot T}{\int_{t_0}^{t_0+T} e^{b \cdot \widehat{V}_{in} cos(\omega_0 t)}} \cdot e^{b \cdot \widehat{V}_{in} cos(\omega_0 t)} \tag{4.21}$$

The integral can be simplified by using the following approximation:

$$\int_{t_0}^{t_0+T} e^{b \cdot \widehat{V}_{in} cos(\omega_0 t)} dt = \frac{2\pi}{\omega_0} \cdot I_0(b \cdot \widehat{V}_{in}) \tag{4.22}$$

where, I_0 is the first kind modified Bessel function of integer order 0. Details concerning the modified Bessel functions of the first kind, please refer to Appendix A. For a large $b \cdot \widehat{V}_{in}$, the following asymptotic approximation holds:

$$I_0(x) = \frac{e^x}{\sqrt{2\pi x}}[1 + \frac{1}{8x}(1 + \frac{9}{2(8x)}(1 + \frac{25}{3(8x)}(1 + ...)))] \tag{4.23}$$

Since $b \cdot \widehat{V}_{in} \gg 1$, Eqn.(4.22) can be further simplified as:

$$T \cdot I_0(b \cdot \widehat{V}_{in}) = \frac{T}{\sqrt{2\pi b \widehat{V}_{in}}} \cdot e^{b \cdot \widehat{V}_{in}} = K(\widehat{V}_{in}) \tag{4.24}$$

Finally, the drain-source current of M_{N2} in strong inversion and subthreshold region is written as a function of the load current:

$$I_{R,S,N2} = \frac{I_{load}^{eff}}{K(\widehat{V}_{in})} \cdot e^{b \cdot \widehat{V}_{in} cos(\omega_0 t)} \tag{4.25}$$

4.3 Input Resistance, Voltage/Power Sensitivity

4.3.1 Voltage Sensitivity

Voltage sensitivity of the power harvester is the minimum voltage amplitude of the RF signal at the input to achieve a certain DC voltage and current supply at the output. The output voltage will be used as the supply voltage of the digital section of the transponder. In this application, the output voltage is fixed at $0.5V$, and the value is chosen to be slightly bigger than the threshold voltage of the transistor so that the digital section works properly with less dynamic power consumption. With substituting (4.24) to (4.19):

$$\widehat{V}_{in} = \frac{e^{2b\widehat{V}_{in}}}{2\pi b \cdot K_2^2(I_{load}^{eff})} \tag{4.26}$$

where $K_2(I_{load}^{eff})$ equals:

$$K_2(I_{load}^{eff}) = \frac{I_{load}^{eff}}{a \cdot \frac{W}{W_0} \cdot e^{x-yV_{out}} \cdot e^{-\frac{bV_{out}}{2N}}} \tag{4.27}$$

The voltage sensitivity depends on the stage number N, the transistor size W as well as the load current. The voltage sensitivity can be found by solving the (4.26) with numerical iterations. Fig.4.7 shows the calculated voltage sensitivity of the power harvester as a function of load currents for different stage numbers and transistor widths. It can be seen that the minimum voltage required to achieve certain DC voltage and current supply is getting smaller with the increase of the number of stages as well as the transistor width. However, the voltage sensitivity improves much slower when the stage number is larger than 6 and the transistor size larger than $7\mu m$. The voltage sensitivity gets worse when the load current increases.

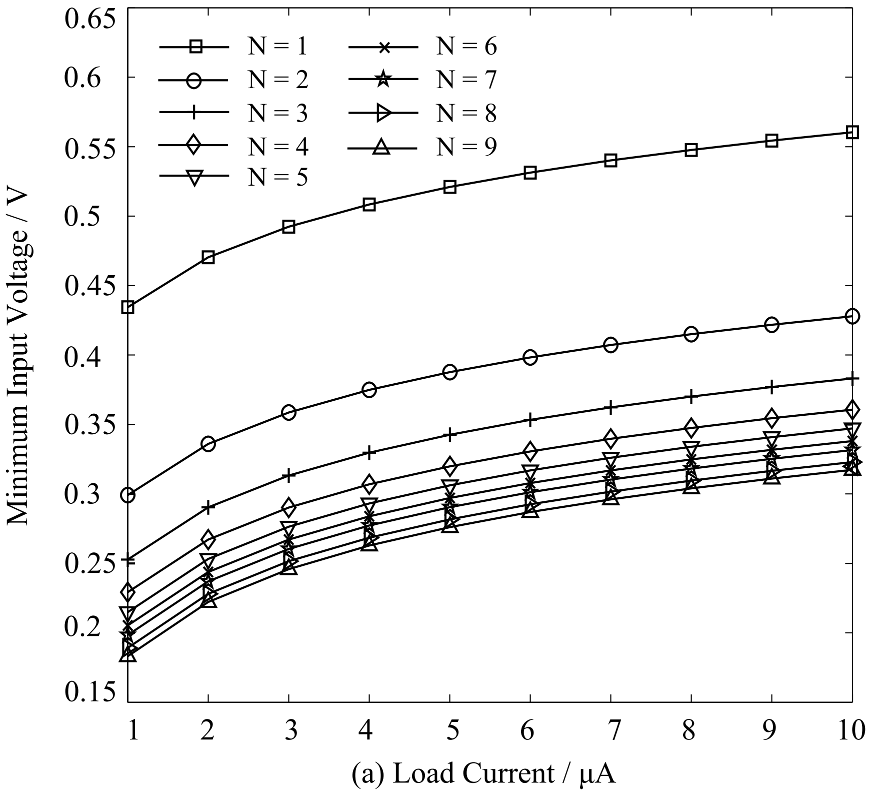
4.3.2 Input Resistance

When M_{N2} works in strong inversion or subthreshold region, M_{N1} is in reverse region and has a reverse current with same direction as $I_{R,S,N2}$. The expression of $I_{R,S,N2}$ is modified by including the reverse leakage current of $M_{N,1}$ as part of the effective load current. The in-phase current of the N-th doubler $I_{R,N}$ which is the summation of $I_{R,N1}$ and $I_{R,N2}$ can be expressed as:

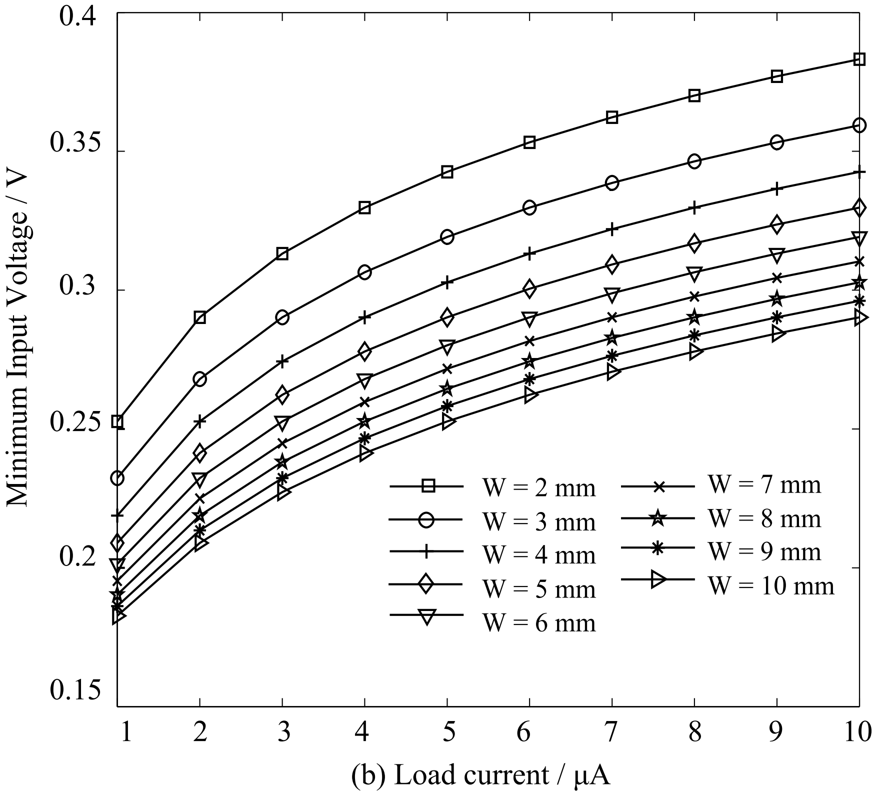
$$I_{R,N} = \frac{I_{load}^{eff}}{K(\widehat{V}_{in})} \cdot (e^{b \cdot \widehat{V}_{in} cos(\omega_0 t)} - e^{-b \cdot \widehat{V}_{in} cos(\omega_0 t)}) \tag{4.28}$$

The analytical expression for input resistance of N-stage rectifier R_{in} is found by substituting (13) to (2):

$$R_{in} = \frac{\widehat{V}_{in} \cdot \pi \cdot e^{b\widehat{V}_{in}}}{2N \cdot I_{load}^{eff} \cdot \sqrt{2\pi b \widehat{V}_{in}} \cdot K_1(\widehat{V}_{in})} \tag{4.29}$$



(a) Load Current / µA



(b) Load current / µA

Fig. 4.7: (a) Voltage sensitivity with different number of stages, the transistor width $W = 2\mu m$; (b) Voltage sensitivity with different transistor width, the number of stages $N = 3$.

with $K_1(\widehat{V}_{in})$:

$$K_1(\widehat{V}_{in}) = \int_{-\pi}^{\pi} cos(x) \cdot e^{b\widehat{V}_{in} \cdot cos(x)} dx \tag{4.30}$$

To verify the resistance model, the power harvesting circuits with different number of stages and transistor sizes were designed based on UMC 0.13-μm technology. The resistance at the fundamental frequency was calculated and compared with the results achieved by large-signal S-parameter (LSSP) simulation in ADS, as shown in Fig.4.8. The input resistance decreases greatly with the increase of the load current consumption, and with a fixed matching network designed for the maximum load current, large return loss is expected in other load currents and hence bad power transfer efficiency.

4.3.3 Power Sensitivity

The power sensitivity of the power harvester is the minimum RF power, which is required at the input of the rectifier, to achieve a certain DC power supply at the output [102]. And the power sensitivity of the circuit can be calculated with the voltage sensitivity and the input resistance as:

$$P_{in} = \frac{\widehat{V}_{in}^2}{2R_{in}} \tag{4.31}$$

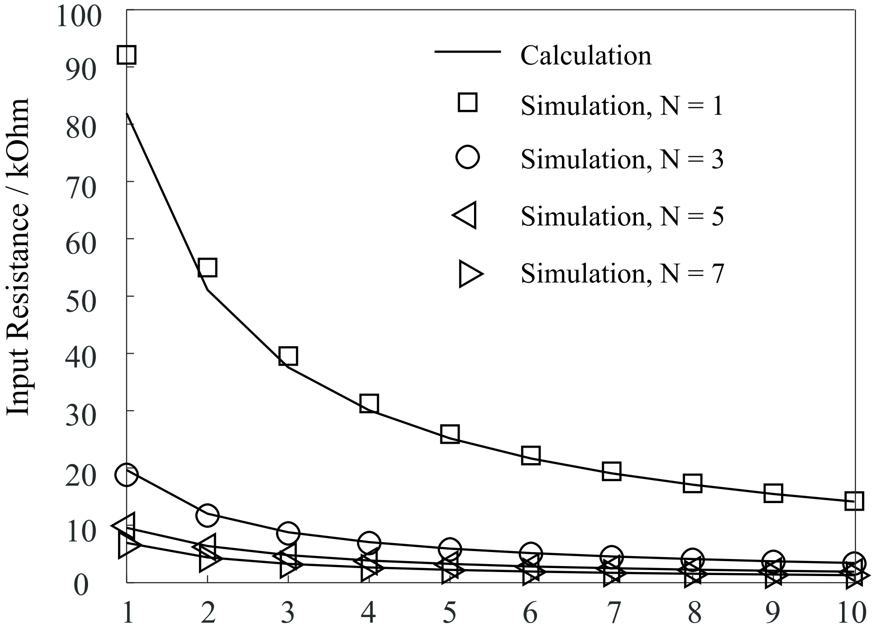
By substituting (4.29) to (4.31), the power sensitivity is expressed as:

$$P_{in} = \frac{\widehat{V}_{in} \cdot 2N \cdot I_{load}^{eff} \cdot \sqrt{2\pi b \widehat{V}_{in}} \cdot K_1(\widehat{V}_{in})}{\pi \cdot e^{b\widehat{V}_{in}}} \tag{4.32}$$

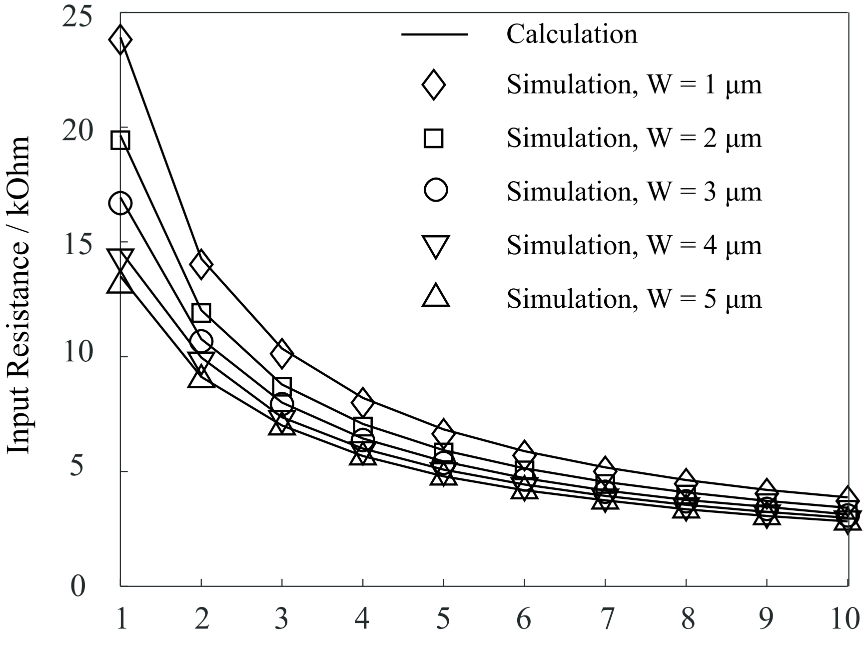
After the voltage sensitivity is found in the numerical way, the power sensitivity of the circuit can be solved with (4.32). Fig.4.9 shows the variation of the power sensitivity. The modelling results are compared with the simulation results from ADS LSSP, and the comparison shows a very good agreement. The minimum required power increases with the increase of the load current demand, the minimum power required changes over 10dB as the load current increases from $1\mu A$ to $10\mu A$.

4.4 Optimal Matching Network

For a 3-stage rectifier with a transistor width $W = 3\mu m$, the input resistance changes from $19.28k\Omega$ to $3.32k\Omega$, and the power sensitivity changes from -27.8dBm to -16.63dBm, as the load current increases from $1\mu A$ to $10\mu A$. A fixed matching network is designed with the input resistance in the case where the load current is maximal, which in this design equals $3.32k\Omega$, and the received power has to be larger than the power sensitivity for obtaining a maximum load current, which is -16.63dBm. However, the overall power conversion efficiency (including the power transfer efficiency of the matching network [17]) drops at other current loads, e.g. from 30.1% to 2.3% as load current decreases from $10\mu A$

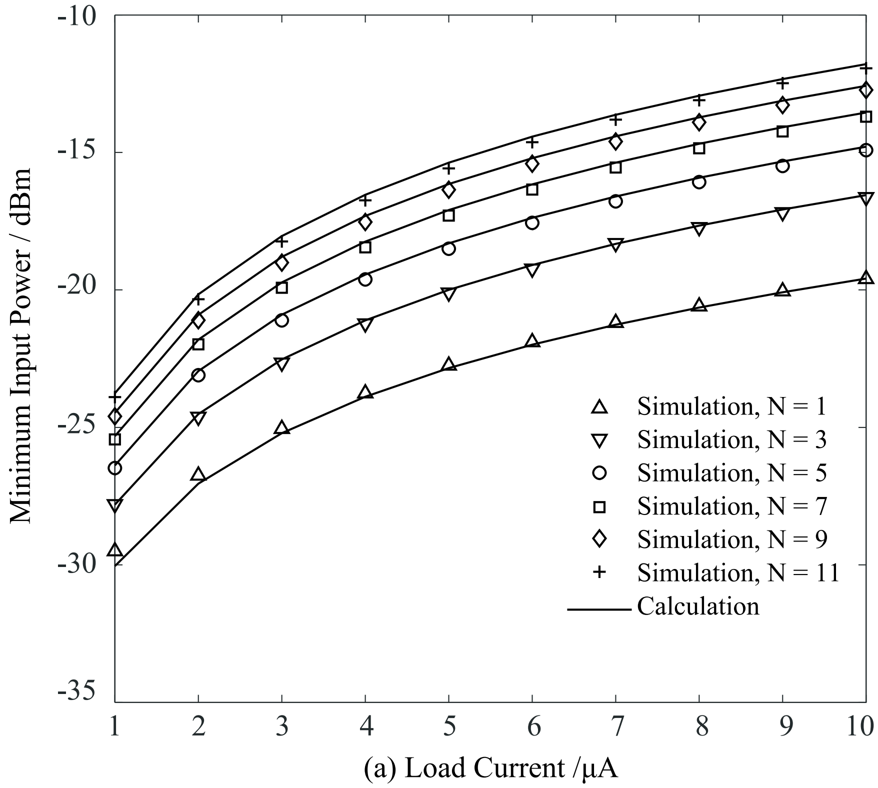


(a) Load Current / µA



(b) Load Current / µA

Fig. 4.8: (a) Input resistance with different number of stages, transistor width $W = 2\mu m$; (b) Input resistance with different transistor width, number of stages is $N = 3$.



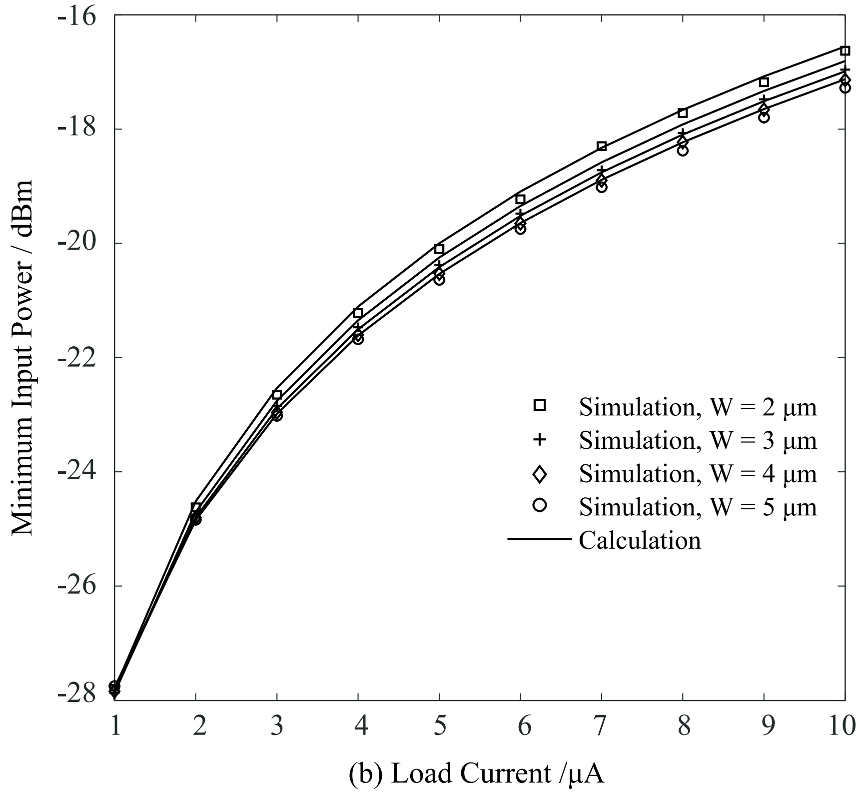


Fig. 4.9: (a) Power sensitivity with different stage number, the transistor width $W = 2\mu m$; (b) Power sensitivity with different transistor width, the number of stages $N = 3$.

to $1\mu A$.
To utilize the power efficiently, it is suggested to tune the matching network based on the load current in order to ensure the maximum efficiency for all operations. In this design, an L-shape downward impedance transformer is applied, and the values of the inductor and capacitor are varied adaptively to ensure the maximum power transfer for all load currents with constant output DC voltage. The tune of the capacitance and inductance is shown in Fig.4.10. To realize the tune of the inductor, a tuneable capacitor is suggested to be used, as shown in Fig.4.2. Possible candidates for tuneable capacitor can be MOS varactor or thin-film varactor based on ferroelectric material, like BST. High-order rectifier is in general preferable with practically realizable capacitance and inductance in IC technology and acceptable consumed die area. However, the power sensitivity gets worse with a larger number of stages, which leads to a tradeoff for circuit design.

4.5 Proposed Energy Harvester

4.5.1 Circuit Design

The proposed energy harvester design is depicted in Fig.4.11. To realize control of the adaptive matching network, supplemental circuitry is designed to sense the load current and further generate the control signal. Another problem arises at the power up phase of the power harvesting. The output DC voltage is not high and steady sufficient to provide the power supply for the control circuitry. When the load current of the rectifier changes, the mismatch happens at the input of the rectifier, and the output voltage of the rectifier may drop such drastically that the power supply is not sufficient for the feedback control circuitry. Therefore, additional design is needed to obtain a steady voltage, which is not influenced by the change of the load current, to provide the power supply for the control circuitry. Inspired by the threshold-voltage cancellation technique proposed in [33], an auxiliary rectifier is designed to provide the DC supply for the feedback control circuit. To provide a steady and sufficient voltage, the load current consumption of the auxiliary rectifier must be much smaller than that of the main rectifier, such that only small amount of RF power is required at the input of the auxiliary rectifier to obtain a sufficient DC voltage. In this demonstration, the main rectifier has a load resistance ranging from 2.5KΩ to 50KΩ. In the following sections, the design parameters of the control circuitry and the auxiliary rectifier will be described.

4.5.1.1 Feedback Control Circuitry

As shown in Fig.4.11, the feedback control circuitry includes a voltage limiter, a voltage reference, a voltage comparator, a sensing resistor and a voltage amplifier. The voltage limiter, which follows the auxiliary rectifier, is designed to bypass the excessive current when the output voltage is larger than the desired value 1.2V in order to avoid the voltage overdrive. The voltage reference generates a steady voltage of around 0.46V in spite of the variance of the supply voltage, and the reference voltage is used for comparison with the amplified sensing voltage. The voltage amplifier is designed to sense the load current with the aid of a small sense resistor. The amplifier works in the linear region instead of the saturation region. Therefore, the output voltage increases linearly with the increase of the differential input voltage. To keep the power consumed by the sense resistor low, small resistor value is preferred; but the voltage over the resistor must locate in the linear input range of the amplifier and be large enough so that the amplified voltage can be distinguished. In this work, the sensing resistor is chosen with a value of 15Ω.

4.5.1.2 Auxiliary Rectifier

The input impedance of the proposed rectifier is the shunt connection of the input impedance of the main rectifier and that of the auxiliary rectifier. The input equivalent capacitance is increased with a value of around 390fF for both load states. The effect on the input resistance when load resistance of the main rectifier equals to 50KΩ is larger than when 2.5KΩ, for the auxiliary rectifier has a large input resistance due to its low output current, which is close to the input resistance of the main rectifier when R_L equals to 50KΩ.

The matching network is designed as an L-shaped highpass matching network. To tune the matching network, both switched capacitor and MOS varactor are possible candidates. Using switched capacitor to adjust the matching network, the design tradeoff between on and off states of the MOSFET switch must be taken in to account. If the transistor is too small, the on-resistance is then very big, and high power loss in the matching network is resulted. If the transistor is too big, the on-resistance is small. However, the capacitance between drain and source/substrate is big, and the isolation between source and drain is lowered due to the capacitive coupling. MOS Varactor holds both good quality factor and high tuning range. However, it is very sensitive to the variation of the control voltage, especially in batteryless system where the feedback control signal strongly depends on the incident power level. In the present work, switched capacitor is employed by using RF MOSFET as switch. To balance the design tradeoff and to improve the isolation in off state, the auxiliary rectifier is designed symmetrically to generate both positive and negative control voltages.

4.5.2 Results and Analysis

The power harvester is designed in a 0.13-μm CMOS process. The post-layout designed for fabrication is shown in Fig.4.12. The inductor is not integrated on chip, and external shunt inductor is chosen from MuRata for test bench. The following presented result and analysis are based on the post-layout simulation.

Tab.4.3 lists the static current consumption of the feedback control circuitry when resistive load of the main rectifier equals to 50KΩ and 2.5KΩ respectively. It can be seen that the bypass current is dominant when load current of the main rectifier is high. The reason is due to the high RF input the voltage limiter starts working to protect the circuit from overdrive by conducting the excess current to ground. The load current consumption of the auxiliary rectifier is 10.43% and 11.38% of that of the main rectifier respectively. The main dynamic current consumption is from the comparator and the output inverter, when the feedback control signals V_{ns} and V_{np} have state transition. Depending on the application, the load status varies quite slowly, therefore, the dynamic power consumption caused by the logic transition can be ignored.

Tab.4.4 summarizes the performance of the designed power harvester with the following figures of merits: the power sensitivity of the rectifier with using the proposed matching network for both load conditions, the output DC voltage of the main rectifier as well as the feedback control signal.

Tab. 4.3: Static Current Consumption of the Control Circuitry

Auxiliary Rectifier Load Current	Resistive Load	
	R_L = 50KΩ	R_L = 2.5KΩ
Voltage Limiter	90nA	17.97μA
Voltage Reference	0.36μA	0.5μA
Amplifier	0.59μA	1.72μA
Comparator	0.18μA	2.57μA
Main Rectifier Load Current	11.7μA	200μA

The performance of the proposed design is compared with the conventional design using fixed matching network from the following aspects: the power transfer efficiency and the overall power conversion efficiency (including the return and insertion loss caused by the matching network) and the comparison result are shown in Fig.4.14 and Fig.4.15. For fixed matching network, two cases are considered: in case I, the matching network is designed for a load of 2.5KΩ and mismatch happens when the rectifier has a load of 50KΩ;

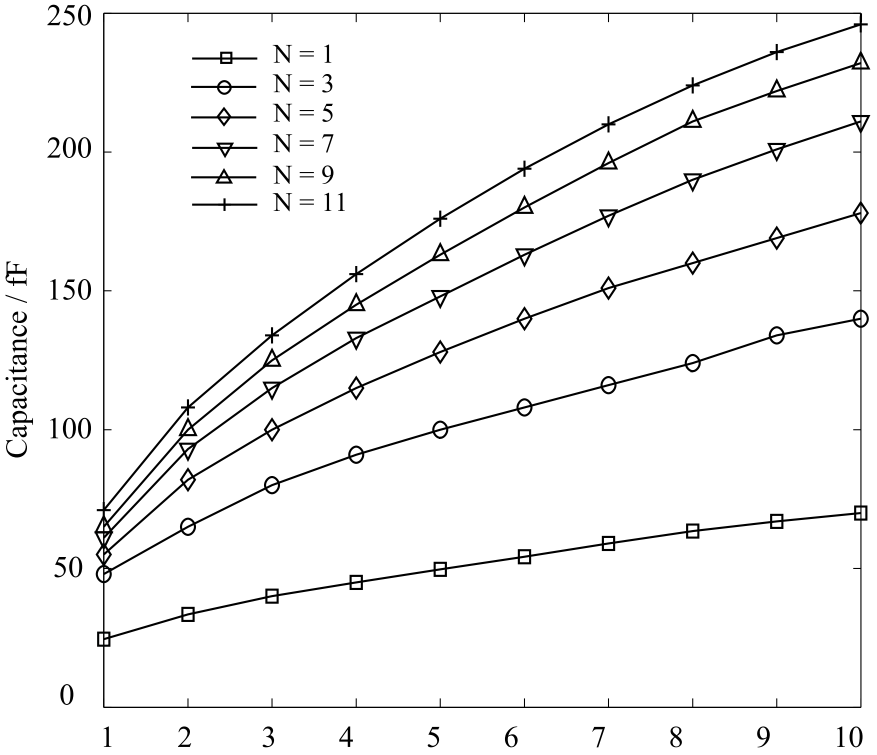
Tab. 4.4: Summary of Power Harvester Performance

Figure of Merit	Resistive Load	
	R_L = 50KΩ	R_L = 2.5KΩ
Incident Power	-7.39 dBm	1.48dBm
Transferred Power	-8.66 dBm	0.37dBm
Output DC Voltage	0.59 V	0.5 V
Feedback Control V_{ns}	-0.88 V	1.08 V
Feedback Control V_{np}	0.69 V	-1.1 V
Reference Voltage V_{ref}	0.44 V	0.48 V

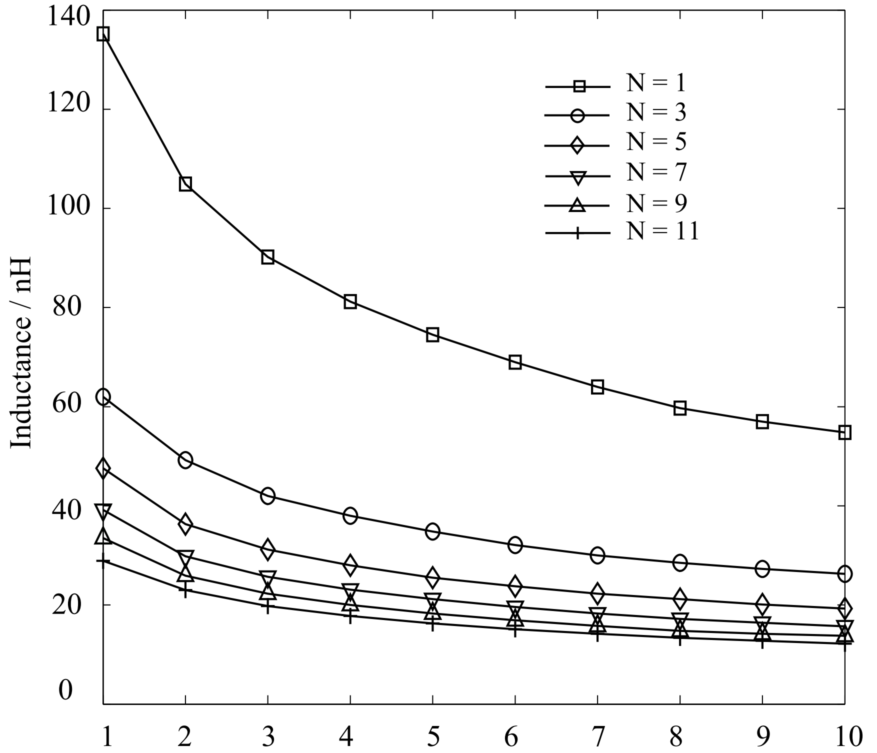
in case II, the matching network is designed for a load of 50KΩ and mismatch happens when the rectifier has a load of 2.5KΩ.
From Fig.4.14, it can be seen that with employing the proposed matching network, the power transfer efficiency is better balanced, comparing with the conventional design using fixed matching network. The power transfer efficiency can achieve a level of over 70%, which is largely improved comparing with the mismatch situations. The overall conversion efficiency is also improved but with a smaller scale depending on the load conditions, as shown in Fig.4.15. The reason is the extra current consumption induced by the auxiliary rectifier and the supplemental control circuitry. However, the benefit of employing the tuneable matching network is distinct even though extra power consumption is introduced in order to improve the power transfer efficiency.

4.6 Summary

In this chapter, the analysis of the RF-DC power harvester with dynamic loads has been focused and a new approach is investigated by adjusting the RF matching network according to the operation conditions with the aid of a feedback control. A compact I/V model of diode-connected transistors working in strong-inversion and subthreshold is developed, with the objective to simplify the analysis. Based on the model, the voltage sensitivity of the circuit is derived and analyzed. A load-dependent large-signal input resistance model and the minimum power required to achieve a certain DC voltage supply with variable load currents are then derived. The concept of an operation-controlled tuneable matching network is proposed in order to maximize the overall power efficiency. Based on the theoretical analysis, a prototype implementation of an energy harvester with the capability of self-adjusting the matching network to adapt to changing load conditions is realized. An auxiliary charge-pump is designed to supply the power for the supplemental control unit. The design is implemented in a standard 0.13-μm CMOS process. The prototype design is analysed based on its post-layout simulation. The results show that the power transfer efficiency with using the proposed design can achieve a level of over 70% independent of the load conditions, which indicates that the power transfer efficiency in variable operation states can be guaranteed with employing the autonomously adaptive matching network.



(a) Load Current / μA



(b) Load Current / μA

Fig. 4.10: (a) The capacitance tune with different number of stages in L-match, and the transistor width $W = 2\mu m$; (b) The inductance tune with different number of stages in L-match, and the transistor width $W = 2\mu m$.

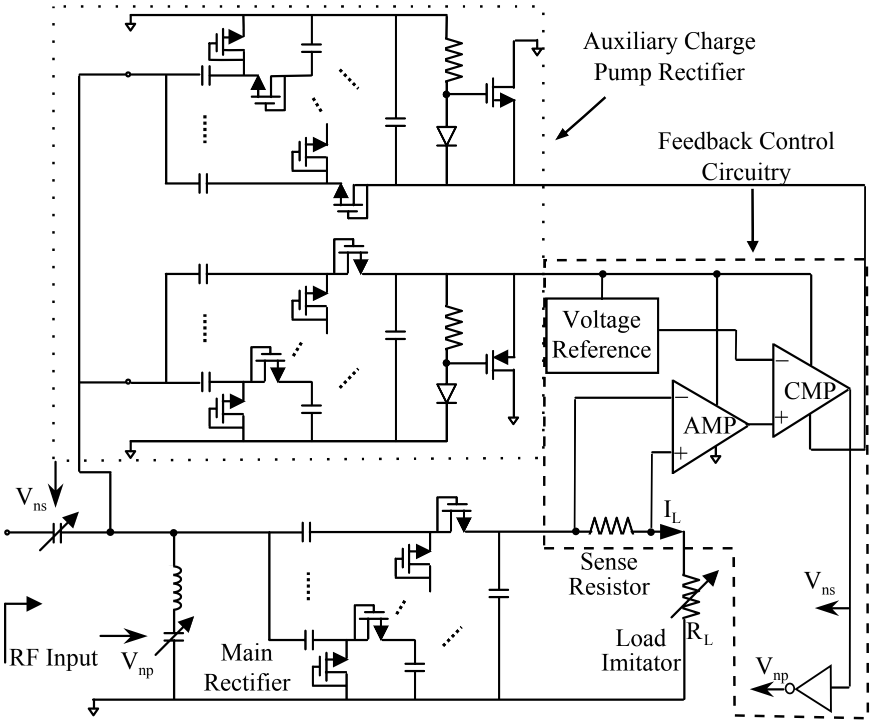


Fig. 4.11: Proposed RF Energy Harvester

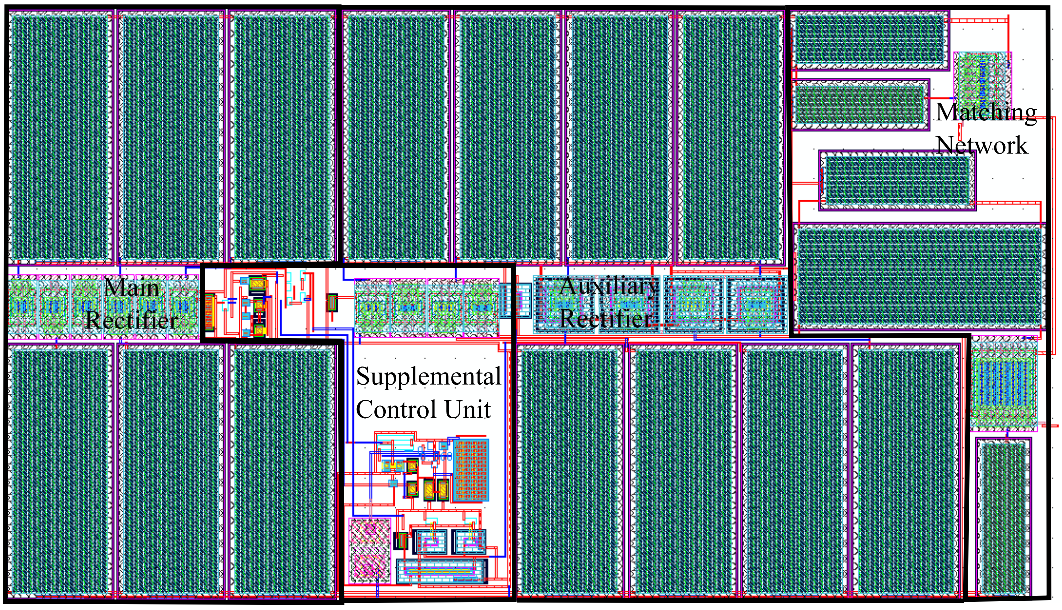


Fig. 4.12: Layout of the Proposed RF Energy Harvester

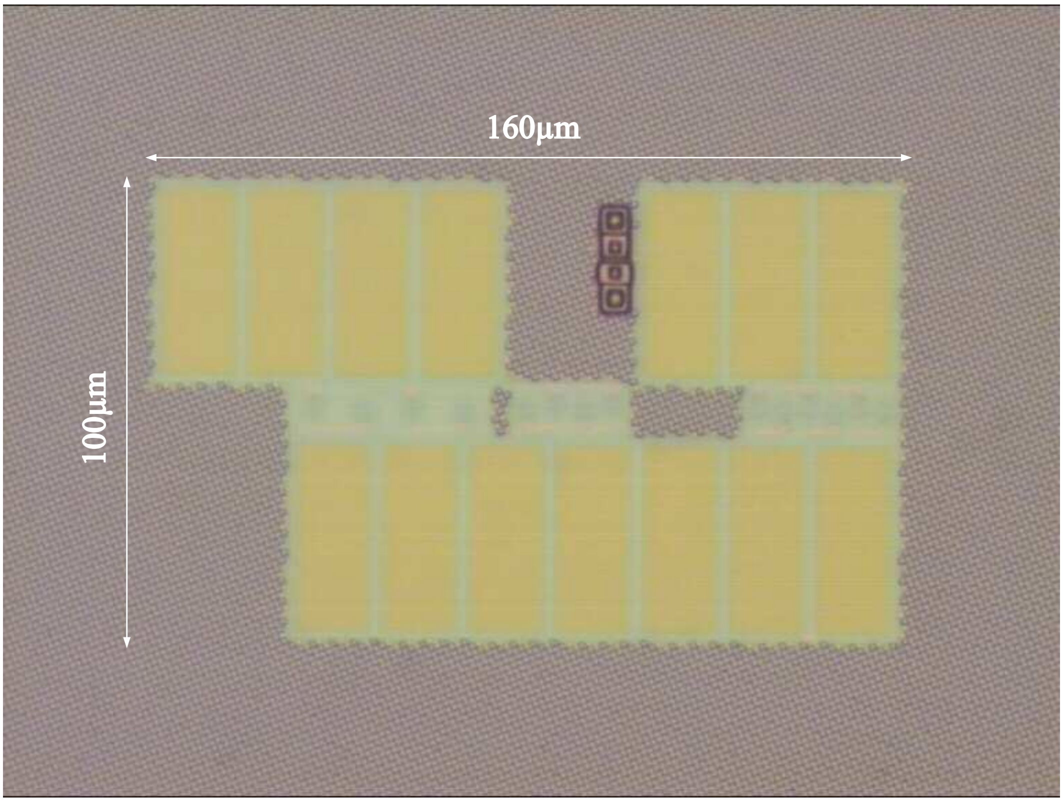


Fig. 4.13: Chip Photography of the Proposed RF Energy Harvester

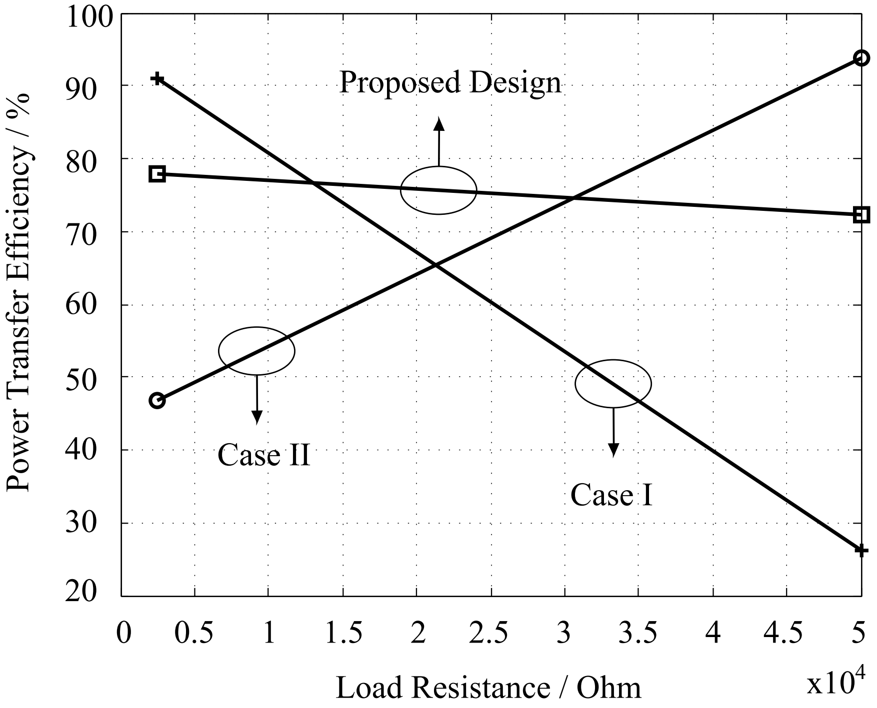


Fig. 4.14: Power Transfer Efficiency

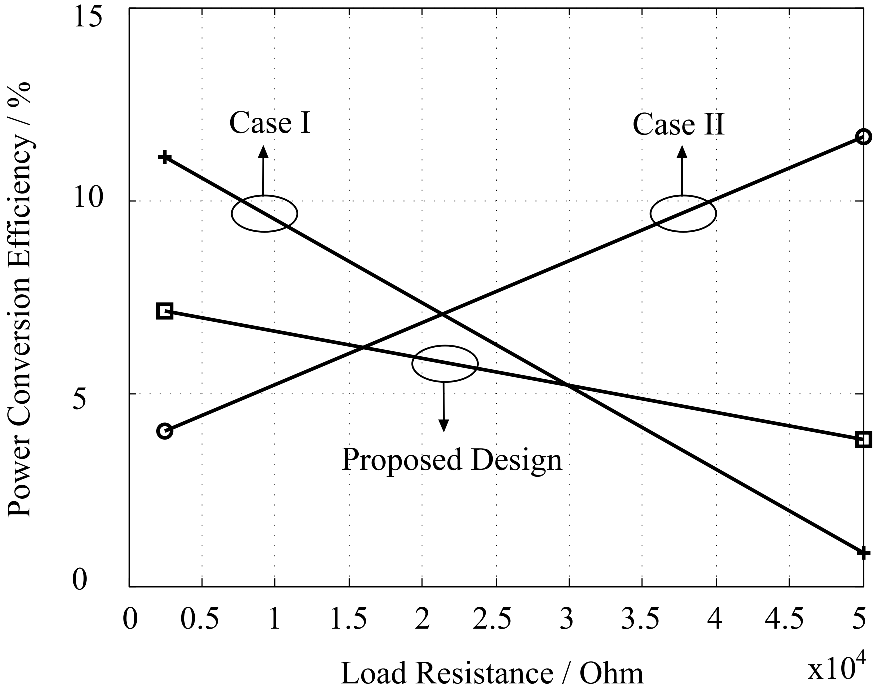


Fig. 4.15: Power Conversion Efficiency

Chapter 5

A Technique of Accelerating the Charging Process of RF Energy Harvester

Contents

This section has been focusing on the RF/DC converter (rectifier) design used for wireless energy harvesting with observing the charging process aiming to improve the power transfer and speed up the charging process. The state-of-art work on RF/DC rectifier has mainly focused on improving of the sensitivity and the energy conversion efficiency [102, 126]. Currently proposed strategies and techniques are based on the steady-state model of the rectifier [17] with the assumption that the rectifier can achieve at the steady state after charging a small storage capacitor to a certain constant voltage in a short time. These designs are mainly intended for the power recovery in RFID transponders, but not applicable for energy harvesting in WSNs which usually employ a large power storage device, like supercapacitors or L-ion batteries. When charging a heavy capacitive load with wireless energy, the charging speed becomes critical. During the charging period, the input impedance of the rectifier is not a steady value, but varies strongly with the proceeding of the charging phase. In this case, the matching network designed based on the steady-state input impedance of the rectifier cannot any more ensure the performance of the charging phase, which can be evaluated with power transfer efficiency and charging speed.

This section investigates the variation of the input impedance of the RF/DC rectifier over the charging phase and presents a technique to accelerate the charging process of the RF energy harvester. It utilizes an adaptive impedance matching network to stabilize the drift of the high frequency input impedance of the harvester during the charging phase. Higher power transmission from the antenna to the harvester can be achieved in the meantime. The prototype energy harvester was built on a PCB with a heavy capacitive loading. Experiment shows that the time, which is needed for charging a 1F super capacitor loading to the harvester to 2V with 0dBm incident signal at 860MHz, can be reduced by 56.5%. The design will be described in two parts: RF/DC rectifier design for energy harvesting and signal conversion; matching network design, for impedance transformation and ensuring the power transfer.

5.1 Input Impedance of Rectifier During Charging-Up

The input impedance of the charge-pump RF/DC rectifier can be modelled as a shunt connection of a resistor and a capacitor [17], as shown in Fig.5.1. The input impedance depends on the incident power density at the antenna, the load condition of the charge-pump. In the former work [139], an analytical model was developed for the varied input impedance of the charge-pump rectifier after it achieves a steady output voltage while the current consumption of the DC load differs. As depicted in Eqn.(5.1), the analysis has shown that the parallel connected resistor in the equivalent impedance approximately inversely proportional to the load current, and on contrast, the capacitor holds a relatively constant value.

$$R_{in} = \frac{\widehat{V}_{in} \cdot \pi \cdot e^{b\widehat{V}_{in}}}{2N \cdot I_{load}^{eff} \cdot \sqrt{2\pi b\widehat{V}_{in}} \cdot K_1(\widehat{V}_{in})} \tag{5.1}$$

with $K_1(\widehat{V}_{in})$:

$$K_1(\widehat{V}_{in}) = \int_{-\pi}^{\pi} cos(x) \cdot e^{b\widehat{V}_{in} \cdot cos(x)} dx \tag{5.2}$$

where, $I_{Load,eff}$ is the load current of the rectifier with involving the leakage current of the diodes; V_{in} is the input voltage amplitude; N is the stage number of the voltage doublers,

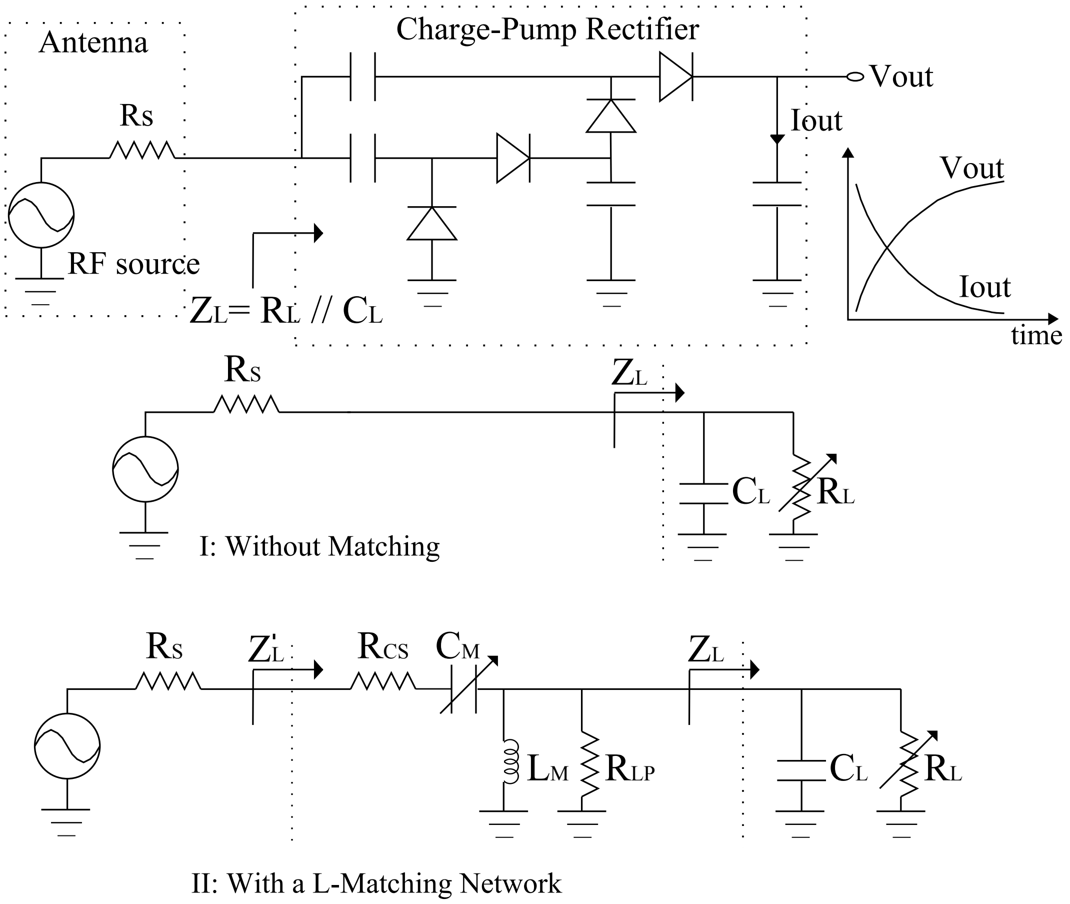


Fig. 5.1: Charge-Pump Rectifier and Equivalent Impedance Transform Circuit

b is a parameter achieved with curve fitting, and is technology-dependent.
Concerning the charging process of the rectifier, the voltage at the load capacitor increases and converges at the final phase. The current flowing to the capacitor decreases significantly, and correspondingly, the in-phase current seen at the input of the rectifier will drastically decrease. The input equivalent shunt resistance will correspondingly increase. To observe the charging process of the RF/DC rectifier, a 2-stage charge-pump rectifier has been designed, with a 1F-super capacitor as the load, as shown in Fig.5.2. Commercial Schottky diode HSMS-286c from AVAGO was used. The prototype design has been developed, and the PCB is shown in Fig.5.2 The input impedance of the designed

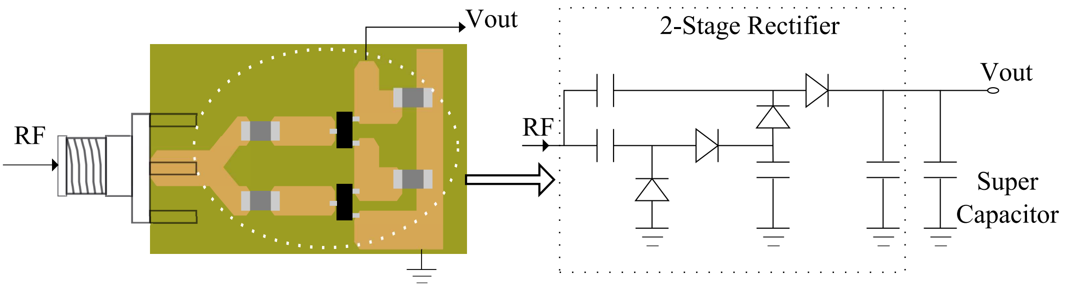
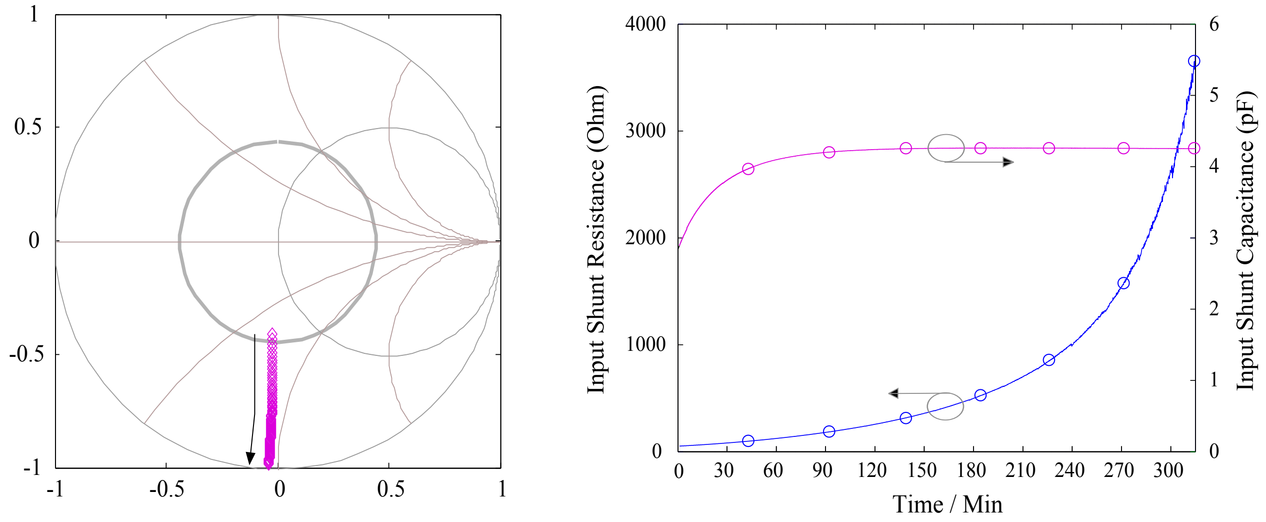


Fig. 5.2: Schematic and Layout Design of the 2-Stage Charge-Pump

rectifier over the charging phase was measured using a network analyzer with reference impedance of 50Ω. The network analyzer outputs an RF signal of 860MHz with the power level at 0dBm. The reflection coefficient is recorded during the charging process, which is then interpreted into equivalent shunt connected resistance and capacitance, as shown in Fig.5.3. It can be seen that, at the starting phase, the parallel resistor holds a low value, and it rises significantly as the load capacitor is charged, while the shunt capacitor varies relatively slightly during the charging phase. The absolute reflection coefficient increases during the charging phase, and the return loss decreases drastically.



(a) The Shift of the Input Complex Impedance over Charging Up Process

(b) The change of the Input Shunt Resistance and Capacitance

Fig. 5.3: Measured Variation of Reflection Coefficient and Input Equivalent Shunt Resistance/Capacitance Over the Charging Process

5.2 Tunable Impedance Matching Network

5.2.1 Application Scope

Impedance matching network has been widely applied in RF/microwave frontends to match the antenna and the RF frontends to improve the power transfer efficiency in conventional wireless communications. In reality, the impedance of the resonating antenna is varied by the change of the surrounding environment. For example, the input impedance of a hand-held antenna alters much from the input impedance tested when putting the antenna on a metal desk. Traditional fixed matching network is designed to match a certain antenna impedance to the RF frontend and keep the transmission loss low when the antenna impedance varies slightly. To compensate the large impedance mismatch between the antenna and RF frontends transmission line, the tunable matching network, which can self-adapt to the surrounding environment, is desirable. A feedback controller can be applied to detect the impedance mismatch by measuring the reflection coefficient at the interface or testing the transmit power gain, based on which, generate a proper DC voltage for the electrically tunable devices, like varactors, as shown in Fig.5.4.

Furthermore, the input impedance of the antenna also changes with the frequency. Next generation of wireless communication systems is being developed for supporting multiple frequency bands and operation modes which are defined in worldwide standards. Addition to the reconfigurability in baseband signal processing, frequency-agile RF frontend is required to cope with the diverse standard definitions. Simply integrating the hardware for specific frequency bands on a single circuit board would largely increase space requirement, design complexity, material cost and the power consumption of the design. Multiband tunable antenna and tunable bandpass filters are desirable to fulfill the demand on miniaturization, low cost and low power consumption. Tunable matching network is then applicable for stabilizing the input impedance of the antenna over multiple frequency bands.

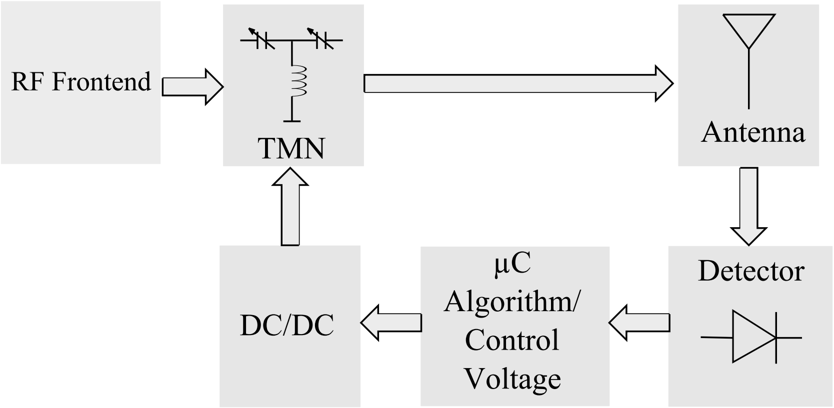


Fig. 5.4: Functional Architecture of Tunable Matching Network with Adaptive Feedback Control

5.2.2 Topologies

Matching networks transform the load impedance to the source impedance for maximizing the power transfer. Topologies with different matching spaces have been developed. For example, for a highpass L-topology matching network, the matching impedance space is shown in Fig.5.5, and by properly choosing the values for static capacitor and inductor in the matching network, the load impedance located in the enclosed region of the brown line can be matched to the reference source impedance. To increase the design degree of freedom, cascading connections of two or more L-topology can be formed as π-match or T-match [63]. To match different load impedances with using a single matching network, a tunable matching network is required by employing tunable capacitors/varactors instead of static capacitors. Typical tunable matching network enlarges the matching region by tuning the varactors. Take the highpass L-topology matching network as an example, as depicted in Fig.5.5, by tuning the varactor, the load impedance on the green curve can be matched with the reference source impedance. By employing a T- or π-topology, the matching region can be extended to an enclosed region by tuning two varactors employed in the network.

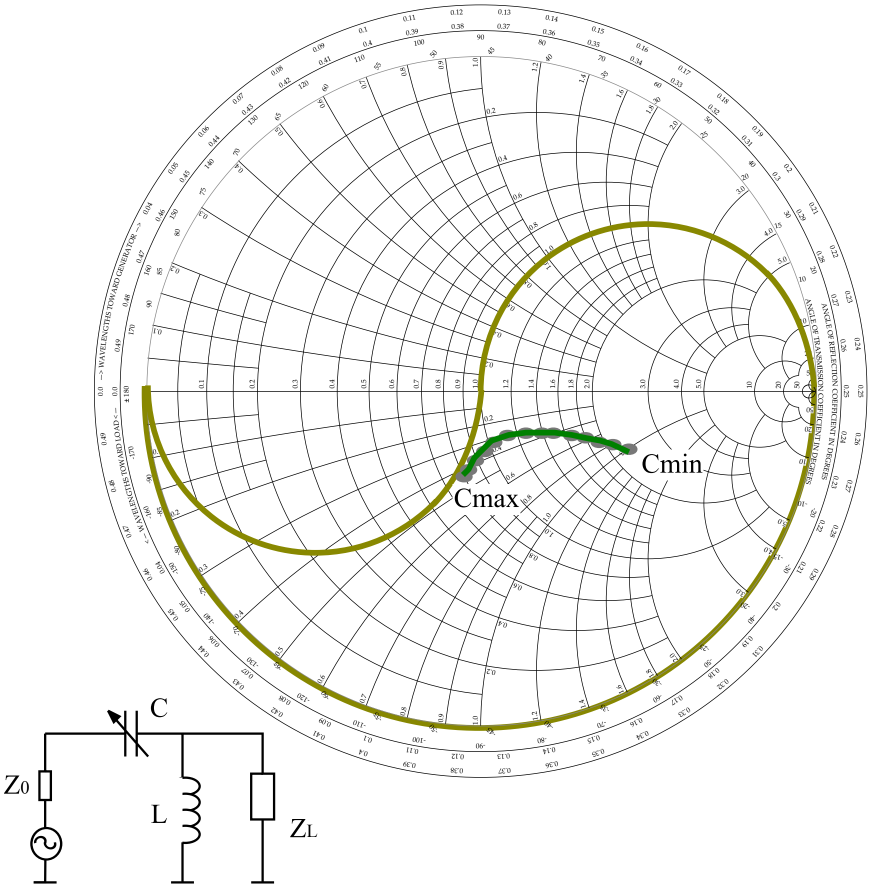


Fig. 5.5: Matching Impedance Space of Highpass L-Match Enclosed in Brown Line; Conjugate Matching Curve of Highpass L-Match in Green Line

5.3 Transient Impedance Matching for RF Energy Transducer

Traditional impedance matching networks are applied in the steady-state process. In this chapter, an innovative application of the tunable matching network in charging procedure of the RF rectifier will be introduced. In contrast to the impedance variation caused by environment change or frequency hopping, the change of the rectifier's impedance during the charging procedure is a transient process.

5.3.1 Theoretical Analysis: Design Guidelines with Lossy L-Match

As shown in Fig.5.3, the input impedance of the rectifier over charging-up procedure locates in the matching space of an L-topology matching network. Therefore, in the following matching network design, the highpass L-match is chosen. By matching the input impedance of the rectifier to the source impedance of the antenna with a lossless L-topology matching network, both the minimum reflection and the maximum power transfer can be achieved simultaneously.

Practically, the matching network is lossy, and the parasitic resistance of the inductor and capacitance shall be taken into account. By employing a matching network, the return loss is improved. However, the power transmitted to the load is not imperatively increased while considering the insertion loss of the matching network. The benefit of employing a matching network will be achieved when the insertion loss induced is less than the improvement of the return loss, or in another word, the transducer gain shall be positive.

As depicted in Fig.5.1, for analysis, cases of both without (I) and with (II) employing a matching network are considered. In case of no matching network between the rectifier and source, the power transmitted to the load P_L can be formulated as:

$$\text{I: } P_L = P_S(1- \mid \Gamma \mid^2) \tag{5.3}$$

where, P_S is the incident power and Γ is the reflection coefficient:

$$\Gamma = \frac{Z_L - R_S}{Z_L + R_S} \tag{5.4}$$

By employing a matching network, the return loss can be improved. Assuming impedance match is achieved at the power input port: $Z_L^{'} = R_S$, the power transmitted to the load is:

$$\text{II: } P_L = P_S(1 - \frac{R_{CS}}{Z_L^{'}})(\frac{R_{LP}}{R_L + R_{LP}}) \tag{5.5}$$

Comparing Eqn.(5.3) and Eqn.(5.5), when the following condition holds:

$$(1 - \frac{R_{CS}}{Z_L^{'}})(\frac{R_{LP}}{R_L + R_{LP}}) > 1- \mid \Gamma \mid^2 \tag{5.6}$$

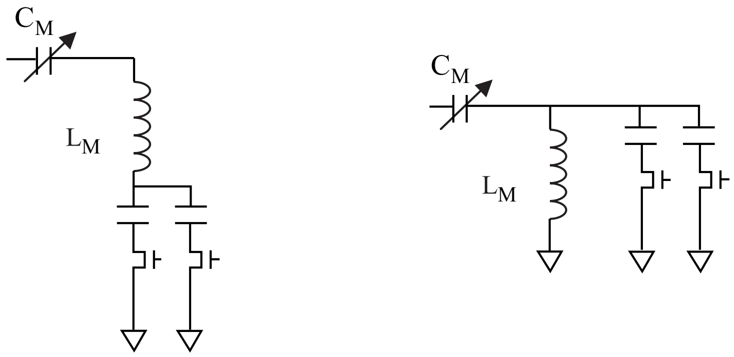
the design will benefit the employment of the matching network by compensating the insertion loss induced by the matching network with the improvement of the return loss. The parasitic resistance of the inductor R_{LP} shall fulfill the following condition:

$$R_{LP} > \frac{R_L(1- \mid \Gamma \mid^2)}{\mid \Gamma \mid^2 - R_{CS}/Z_L^{'}} \tag{5.7}$$

5.3.2 Tune of Inductor

Based on the analysis of the input impedance of the rectifier, to transform the high load impedance to a lower source resistance, an L-topology highpass matching network is employed. The designed matching network is used in wireless power transfer, and in order

a) Inductor with Serial MOS Varactor   b) Inductor with Parallel MOS Varactor



c) Inductor with Serial Switched Capacitor   d) Inductor with Parallel Switched Capacitor

Fig. 5.6: Tune of the Inductor

to keep the communication distance, the power consumption caused by tuning matching network due to the lossy parasitics has to be kept low, and the gain by tuning the matching network is kept. The topologies shown in Fig.5.6 are applicable in the desired matching network, where the switched capacitor and MOS varactor are chosen as possible candidates. The shunt inductor L_M is connected with parallel or serial capacitors. When the value of the capacitor is tuneable, the effective inductance is then changeable. The following sections will discuss how proper topology and tuneable component are chosen. Ideally, serial and parallel connection of capacitor with an inductor shows no difference. However, due to the resistive parasitics existing in inductors, the tuneability of the matching network tradeoff with its self-power consumption. Assuming the inductor has a parasitic serial resistor R_L, the effective impedance of the parallel connection of the capacitor and the inductor can be expressed in the following equation:

$$\begin{aligned} Z = & \quad (j\omega L + R_L)//\tfrac{1}{j\omega C} \\ = & \quad \tfrac{j\omega L(1-\omega^2 LC)-j\omega R_L^2 C}{(1-\omega^2 LC)^2+\omega^2 R_L^2 C^2} + \tfrac{R_L(1-\omega^2 LC)+\omega^2 R_L CL}{(1-\omega^2 LC)^2+\omega^2 R_L^2 C^2} \\ \approx & \quad \tfrac{j\omega L}{1-\omega^2 LC} + \tfrac{R_L}{(1-\omega^2 LC)^2} \end{aligned} \tag{5.8}$$

Please note the approximation is established with condition that the serial resistance of the inductor is small and $(1-\omega^2 LC)$ is positive. Take the following values: L = 5.6nH, C = 0.42pF, $R_L = 2\Omega$, and substitute to the above equation. The effective impedance is then an inductor of 2.27*L with a serial resistor of 5.14*R_L. The example above shows the tradeoff between the tuneablity and the self power consumption of the matching network: while increasing the tuneability, the power consumption of lossy matching network is even more strongly increased. Therefore, in order to keep the profit of employing a tuneable matching network, the parallel connection of the inductor with a varactor or switched capacitor is avoided.

5.3.3 Tuneable Capacitor

Variant technologies have been developed for adaptive RF systems. Based on the processing techniques and design materials, it can be classified in to active and passive technologies, as shown in Fig.5.7, of which, semiconductor based tuneable capacitor are assembled into active group, like MOSFET varactor, switched capacitor, diode varactor; while the ferroeletric-based and micro-electro-mechanical (MEMS)-based products are sorted in to passive group, like BST (Barium Strontium Titanate)-based capacitor. The different techniques can be evaluated in variant figure of merits: linearity, loss, control voltage, integration, manufacture cost, technology maturity. All kind of varactors are possible candidates for realizing the tuneability. However, before choosing one from them and applying in the matching network, it is necessary to examine their RF small signal models. The following sections give a brief introduction and comparison of different techniques.

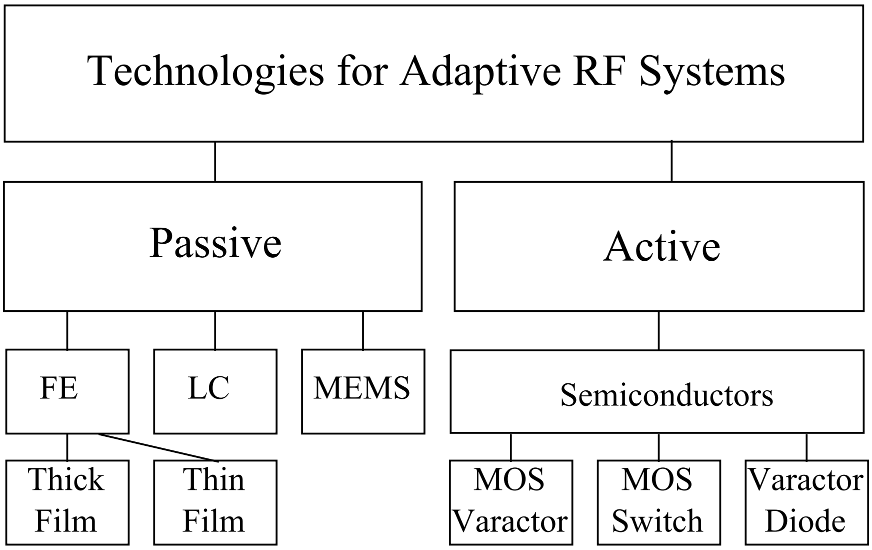
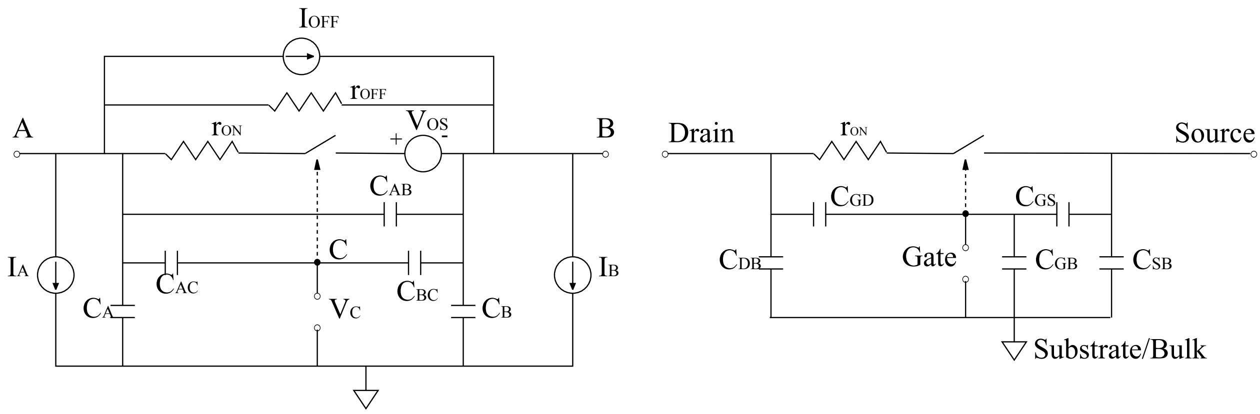


Fig. 5.7: Technologies for Adaptive RF Systems

5.3.3.1 MOSFET Switch

MOSFET can be employed in switched capacitors, which has been used in many applications, e.g. active filters, voltage control oscillators [79] etc.. Due to its availability in standard CMOS technologies, in contrast to other techniques like MEMS or BST based varactors, the control voltage is quite low with the ongoing decrease of power supply voltage in CMOS technologies. The manufacturing cost is largely decreased due to the mass production in mature technologies. The RF model of a MOSFET switch can be simplified as shown in Fig.5.8. To reduce the charge feedthrough caused by the coupling capacitance from the gate to both source and drain, the gate terminal is isolated with AC signal by connecting with a large resistor. In order to avoid the influence of the substrate coupling, the source terminal is suggested to connect to the ground.



(a) Model for a non-ideal switch (b) Model for MOSFET-Switch

Fig. 5.8: (a) A General Model of a Non-ideal Switch [3], where, current sources I_X represents the leakage current; r_{ON} and r_{OFF} are on and off resistances respectively; C_{XY} are the coupling capacitances; V_{OS} is a voltage offset (b) Small Signal Model of a N-channel MOSFET Switch

In the on-state of the switch, the MOSFET works in the non-saturation region; for off-state, the MOSFET works in the cut-off region. For on-state, the current-voltage relationship is modelled as:

$$i_D = \frac{\mu C_{ox} W}{L}[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}] \tag{5.9}$$

where, v_{GS} and v_{DS} are the voltage between gate and source, drain and source terminals, respectively; V_T is the threshold voltage; W, L are the width and length of the MOSFET; μ is charge-carrier effective mobility; C_{ox} is the gate oxide capacitance per unit area. To work in the non-saturation region, the voltage applied to an N-type MOSFET $v_{GS} - V_T$ must be larger than zero and v_{DS}. The on-resistance is given as:

$$r_{ON} = \frac{1}{\partial i_D / \partial v_{DS}} = \frac{L}{\mu C_{ox} W (V_{GS} - V_T - V_{DS})} \tag{5.10}$$

The on-resistance is reduced with the increase of the transistor size W/L, while the capacitance between drain and source/substrate terminals is increased. For on-state, switch with larger W/L is preferred due to its smaller on-resistance which results in lower loss. A MOSFET switch with large transistor size can not realize good isolation between drain and substrate in off-state due to the capacitive coupling. The design tradeoff has to be found to achieve good performance for both on- and off-state.

5.3.3.2 MOS Varactor

Unlike the MOSFET switch, the MOS varactor has an asymmetric structure, as shown in Fig.5.10. MOS varactor is an agile application of a normal MOSFET by using gate as one terminal and combining the source, drain and bulk terminal to form a second terminal. MOS capacitance has four operation regions: accumulation, depletion, weak inversion, and strong inversion, based on the bias voltage applied between the gate and Nwell terminals [96, 116]. A regular MOS does not provide a MOS capacitance which is a monotonic function of the bias voltage, as the dotted line shown in Fig.5.9. To acquire a monotonic function, it is desirable to manufacture an accumulation-mode MOS capacitance (A-MOS) by fabricating the D-S diffusions in an n-well instead of the normal p-substrate for a NMOS varactor [24,71,106]. An alternative is to force the MOSFET working only in inversion mode (I-MOS) by disconnecting D-S terminals and bulk terminal, instead, connecting the bulk to the highest potential for p-type MOSFET or grounding the bulk for n-type MOSFET [4].

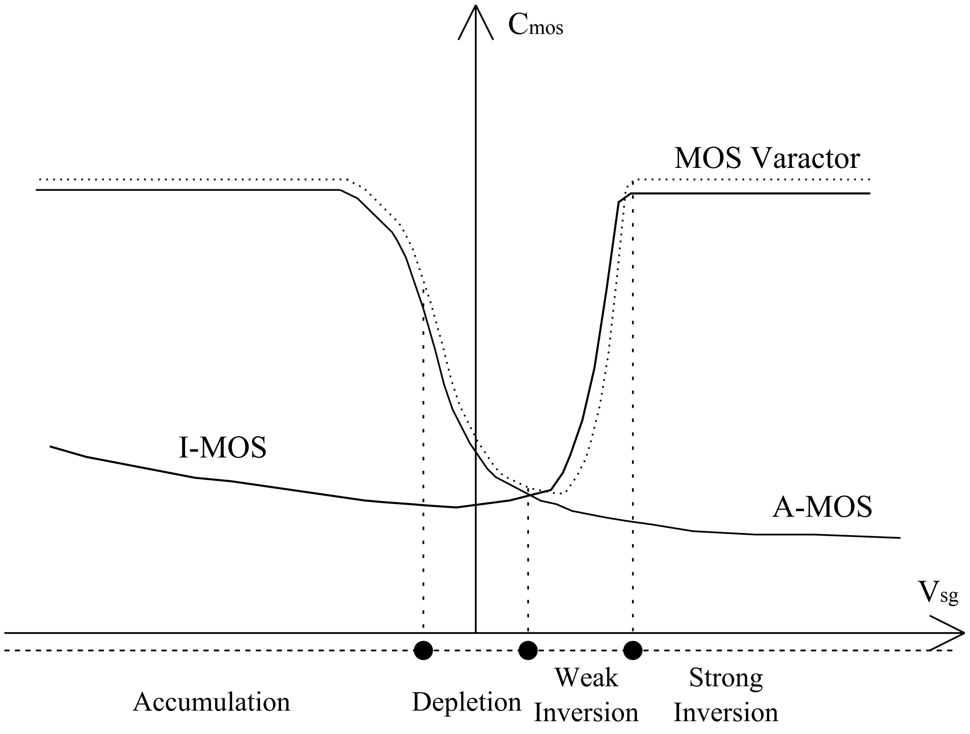


Fig. 5.9: Capacitance Characteristics of a MOSFET

Fig.5.10 depicts the high frequency model of a NMOS varactor. In order to reduce the coupling effect caused by the substrate, the Nwell terminal must be grounded or connected to a load with low impedance. For a MOS varactor with a tuning range up to 4, the quality factor can achieve 80 with bias. However, due to the asymmetric structure in MOS varactors with non-grounded N-well terminals, which transfers the impedance to a smaller value before it couples with the substrate capacitor, the MOS varactors are only applicable when the gate terminal is connected to a small impedance load.

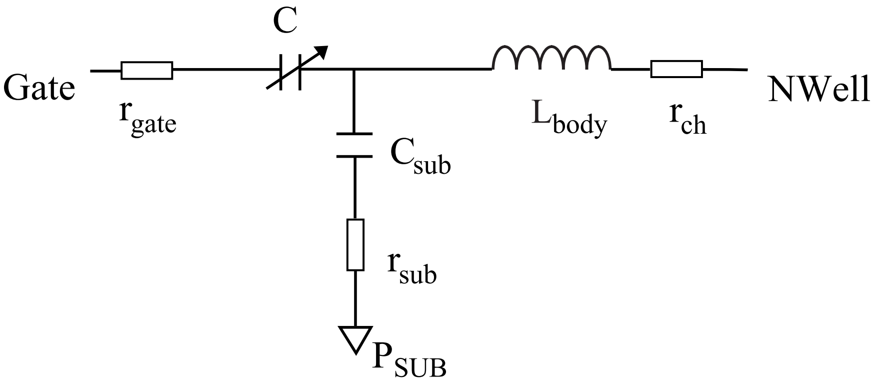


Fig. 5.10: Equivalent Circuit of NMOS Varactor

5.3.3.3 Varactor Diode

Varactor Diode is a semiconductor p-n junction, which can be made of Gallium-Arsenide (GaAs), Silicon (Si) or Silicon-Germanium (SiGe), and has been widely used in adaptive RF circuitries, like voltage-controlled oscillators. By applying a reverse voltage to a diode, the thickness of the depletion layer is varied which results in a changeable capacitance. The small signal model of a varactor diode is shown in Fig.5.11. The low control voltage (usually less than 10V) along with the large tuneability ($> 10 : 1$), as well as the low manufacturing cost, establishes the preponderance of the varactor diodes. The power handling capability is limited due to the low reverse bias voltage. The quality factor is not superior compare to the ferroelectric varactor or MEMS varactors.

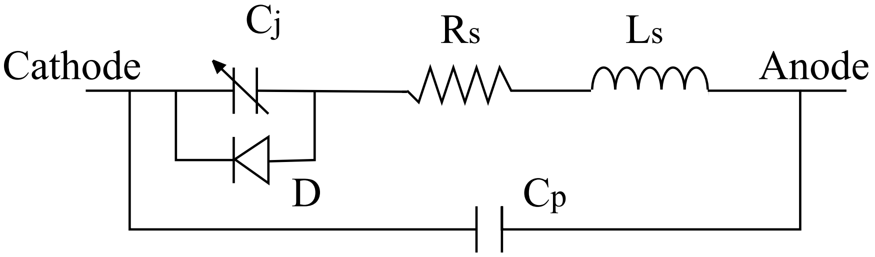
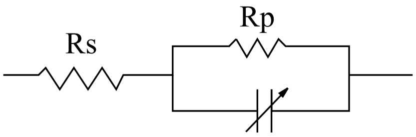


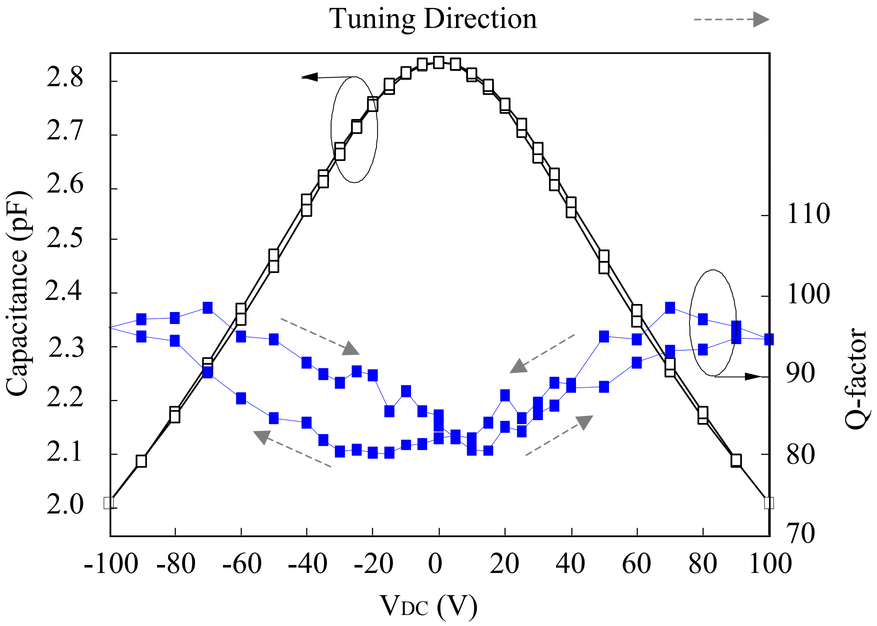
Fig. 5.11: Equivalent Circuit of Varactor Diode: L_p and C_p represent the package parasitics; C_j is the junction capacitance which depends on the applied reverse bias; R_s is the serial resistance

5.3.3.4 Ferroelectric Varactor

Low leakage currents, low loss, high permittivity and simple manufacture process have made the ferroelectric varactors one of the most adequate candidates in the application of tuneable RF and microwave components [38, 133]. Among diverse ferroelectric materials, $Ba_{1-x}Sr_xTiO_3$ (BST), due to its high dielectric constant, high tuneability, low dielectric loss and high breakdown strength, becomes the most investigated ferroelectric material for various applications especially tuneable devices [51]. The equivalent cir-



(a) Equivalent Model of a BST-based Varactor



(b) Capacitance and Q-factor of a Thick-film BST-based Varactor versus Tuning Voltage

Fig. 5.12: (a) Equivalent Circuit of a BST-based Varactor [133], where R_S represents the parasitic conductor and contact resistance; R_P represents the dielectric loss; (b) The Performance of a Thick-film BST-based Varactor [132]

cuit of a BST-based varactor and the performance of a thick-film BST-based varactor are shown in Fig.5.12. BST-based varactor physically holds a symmetric structure which results in an even dependence of the capacitance over the control voltage. Despite of the high linearity and high quality factor, thick-film varactor suffer from a high control voltage which is not applicable in the impedance matching network in RF energy harvesting circuitries. By reducing the thickness of the film, the control voltage can be reduced less than 10V [127, 133].

5.3.3.5 MEMS Varactor

The capacitance of a microelectromechanical system varactor is varied by changing the distance between the capacitor plates with tuning the applied DC control voltage. Due to the high dielectric material, the loss of the varactor is kept very small and hence a high quality factor. Since the distance of the capacitor plates is physically changed with a certain mechanical settling time, the tuning speed is low compared to other technologies. The quality factor of MEMS varactors is high which is much more attractive than silicon varactors for applications in the microwave and millimeter wave [67, 108]. The MEMS varactors also have a symmetric structure, and the varactor can be modelled as a serial or parallel connected RLC network.

5.3.3.6 Comparison of Varactor Technologies

The aforementioned varactor technologies are compared in different figures of merit and summarized in Tab.5.1, with a representative example for each technology.

Tab. 5.1: Comparison of Varactor Technologies

FoM	Silicon Varactor [45]	Thin-Film BST-Based Varactor [108]	MEMS Varactor [67]
Linearity	Low	Medium	High
Tuneability	High	Medium	Low
Q-factor	Low	Medium	High
Manufacture Cost	Low	Low	High
Control Voltage	Low	Medium	High
Power Handling	Poor	Good	Good
Maturity	Advanced	Under research	Under research
Tuning Speed	Fast	Fast	Slow
Integration	High	Medium	Low

5.3.4 Choice of Lump Elements

Analysis has been done to find the performance requirement of the lumped elements L_M and C_M in the matching network. In the analysis, it is assumed that the capacitor C_M has a typical ESR of 1Ω. Sampling the input impedance of the rectifier during the charging phase at different time points, the quality factor of the inductor L_M shall fulfill a certain value to hold the condition in Eqn.(5.7), referring to Tab. 5.2. The required minimum quality factor L_M shall fulfill decreases as the load being charged. At the beginning of the charging phase, the quality factor of L_M shall be larger than 5.19, which is a trivial performance requirement for inductors. For transforming the impedance to the fixed antenna impedance 50Ω, the value of the inductor L_M shall vary slightly during the charging phase due to the small change of the input parallel capacitance of the rectifier. The value of the parallel C_M shall change considerably. By tuning the varactor C_M in the designed

Tab. 5.2: Summary of the theoretically required L_M and C_M at different time points

Time Point / Min	30	90	150	210	270
R_L/Ω	81.6	181	359.6	703.5	1551
C_L/pF	3.81	4.2	4.26	4.26	4.26
$\mid \Gamma \mid$	0.575	0.788	0.887	0.941	0.973
$min(R_{LP})/\Omega$	187.9	118.1	102.7	95.3	91.1
C_M/pF	9.41	5.59	4.75	4.46	4.35
L_M/nH	6.7	5.75	5.61	5.6	5.59
$min(Q_L)$	5.19	3.8	3.39	3.15	3.02

matching network, a high conversion efficiency is maintained during the charging process, and the charging phase is expected to be accelerated.

To simplify the design, a static inductor of fixed value 5.6nH with quality factor above 50 at 860MHz is chosen for L_M. The capacitor shall vary from 9.41pF to 4.35pF for transforming the impedance during the charging phase, which requires a varactor with the tuneability of around 54%. Further, limited by the application environment, the control voltage for tuning the capacitor is up to battery level. Tuneable components are the key to implement the proposed functionalities, where balanced cost-effectiveness is the determining criteria for choosing their realization technology. The employment of the thick-film ferroelectric varactors which usually require a control voltage of around 60 volts [100] is excluded in spite of the high quality factor. The requirement of the tuning range, as well as the control voltage, has reached the performance boundary of the MEMS varactors. Among the existing and emerging technologies, BST thin-film based components have shown a promising performance with its potential high tuning range, affordable manufacturing complexity, cost as well as low control voltage, but since the technology is still under research, no commercial component is currently available. Silicon varactors are superior in low control voltage and large tuning range but suffer a high current loss.

To demonstrate the benefit of employing a tuneable matching network in the charging procedure of the RF energy harvester, a commercial silicon tuning diode BB833 from Infineon Technologies is chosen as C_M. The results have verified that, in spite of the low quality factor of the employed varactor, the charging speed is significantly improved. The schematic and layout design of the experimental board is shown in Fig.5.13. A control signal V_c is emulated with a DC power supply for tuning the varactor. Two DC block capacitors of 100pF are used to block the control signal and a large resistor as RF choke, through which the control signal from a Keithley source meter is applied to the varactor.

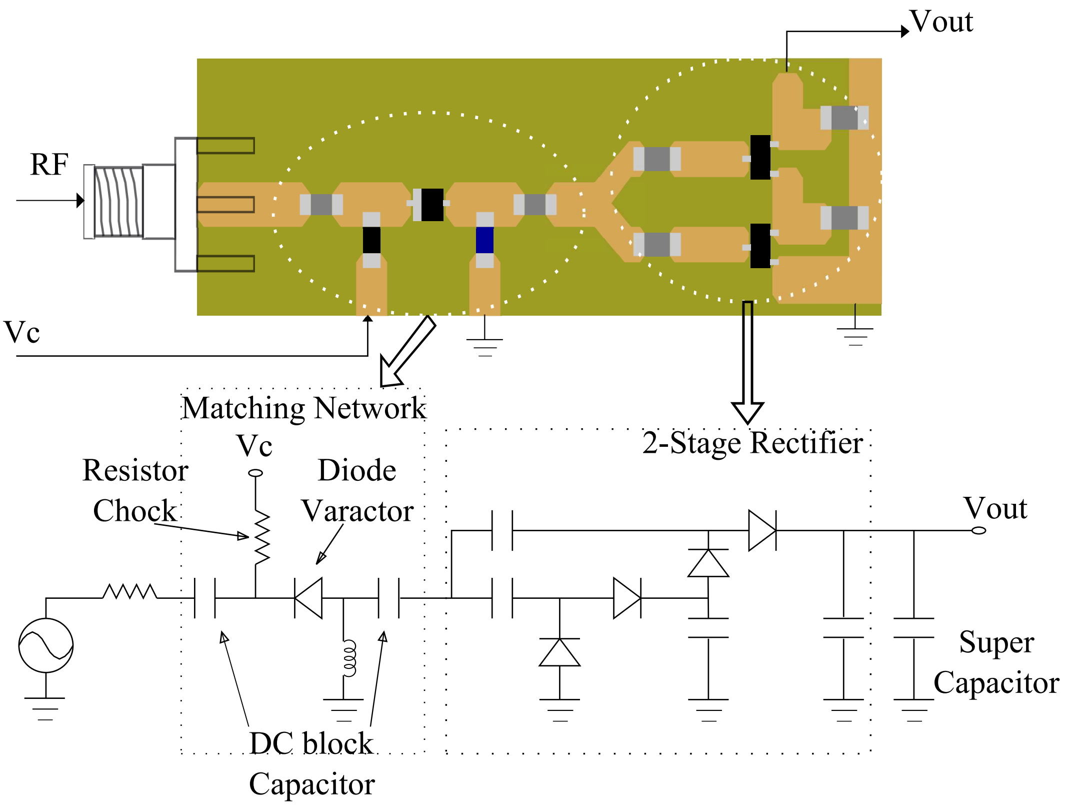


Fig. 5.13: Schematic and Layout Design of the Experimental Board

5.4 Experimental Results

To demonstrate the proposed technique, prototypes of the RF/DC energy harvester with and without adaptive matching network have been designed on PCB. An RF signal of 0dBm at frequency 860MHz from an Anritsu vector network analyzer with internal impedance of 50Ω is used as the input of the energy harvester. The rectifier is loaded with a super capacitor of 1F, and the charging phase is observed with the Anritsu vector network analyzer for measuring the one port reflection coefficient and a data logger for recording the DC output voltage. Fig.5.14 shows the experiment setup. A DC power supply is used as a control voltage to test the harvester with the adaptive matching network.
The results are compared with figure of merit - charging speed in three different cases: I. without matching network; II. with a static matching network designed based on the impedance at the beginning of the charging phase; III. with the proposed adaptive matching network.
Fig.5.15 and 5.16 shows the experimental results. In case I, the rectifier is directly mounted to the power source. As the charging proceeds, the load impedance seen at the source moves to peripheral point in the Smith Chart. Recall the sampled values in Tab. 5.2, the parallel connected equivalent resistor gets larger such that the power transfer reduces. The charging speed is slower comparing with other two cases, and after about 5-hour's charging, the output voltage becomes steady at 1.3V. In case II, a fixed matching network

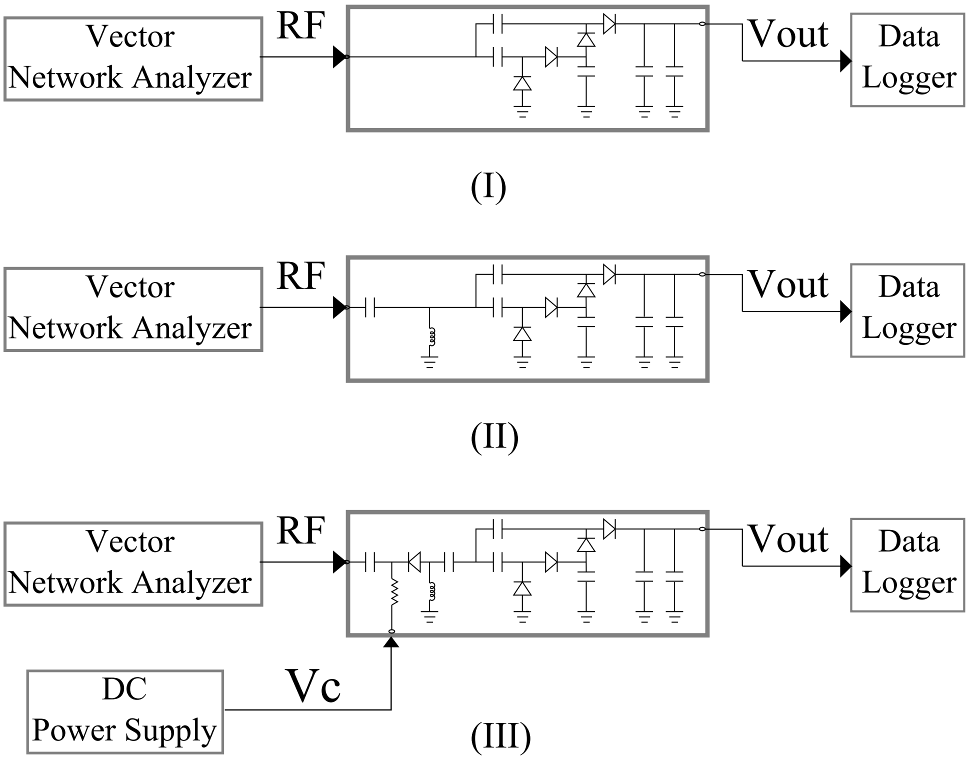


Fig. 5.14: Experimental Setup of Measurement of the Prototype Designs. Three experiments were performed for comparison: (I) the RF source signal is directly sent to the charge-pump; (II) the RF signal is sent to the charge-pump through a static matching network; (III) the RF signal is sent to the charge-pump through an adaptive matching network.

is applied. As the charging phase begins, the load impedance seen at the source is well transformed to the center of the Smith Chart, and the charging speed is improved considerably compared with case I. 67% less time is taken to charge the capacitor to 1V than case I. However, the process slows down after about 1-hour's charging due to the change of the transformed impedance from center to the open circuit point.

Some questions are still open. Tab.5.2 has listed the input impedance of the rectifier as well as the required lumped components for matching the input impedance of the rectifier at different time points, and for a static matching network, the working status is designed according to the input impedance of the rectifier obtained at the initial time point. Therefore, as seen in Fig.5.16, the impedance after the transformation of the static matching network locates in the certer of the Smith Chart when charging procedure starts. After a short time, the impedance seen at the input of the matching network drifts away from the center and new matching is desired. However, the impedance seen at the input of the rectifier alters from the value obtained at the same charging time point in the setup I. The reason is due to the dependence of the input impedance of the rectifier on its working status: output voltage, input power level. Comparing setup I and II, with and without matching network, the rectifier is charged to different output voltage levels after the same charging time, refer to Fig.5.15. However, the input impedance obtained in setup I is still valuable with providing a direction of the adaptive control.

In case III, an adaptive matching network is used. At the beginning of the charging phase, the matching network is tuned to transform the impedance close to the internal impedance of the power source for optimal power transfer. The same phenomenon as in setup II appears: the impedance seen at the power source drifts away from the center of the Smith Chart, and the charging speed slows down as the output voltage starts to converge. Based on the input impedance measured in setup I, a control voltage of 4V is applied to the varactor diode after charging for about 1.3-hour, and the impedance seen at the source is transformed close to the reference impedance. The output voltage shows an abrupt increase after tuning the matching network, which speeds up the charging process significantly. Comparing case II and III, to charge the load capacitor to 2V, by employing the adaptive matching network more than 2 hours can be saved.

The demonstration has proved that by employing an adaptive matching network in RF/DC rectifiers, a high conversion efficiency can be maintained throughout the whole charging process. The charging speed is considerably accelerated with a higher output voltage.

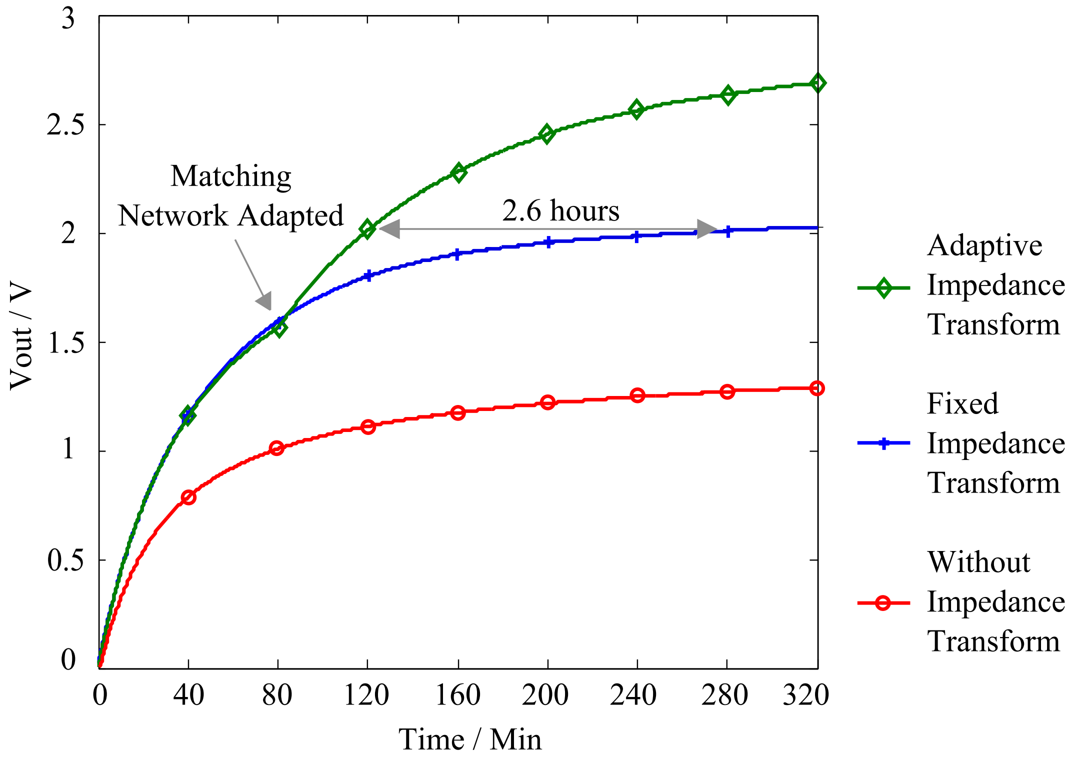


Fig. 5.15: Measured Output Voltage Over the Charging Process with Different Impedance Transform Circuitries

5.5 Adaptive Control

In the current setup, the adaptive control signal is provided by a source meter and tuned manually when the output voltages starts to converge. The input impedance of the rectifier over charging procedure has been tested in experiment setup I. The experiment

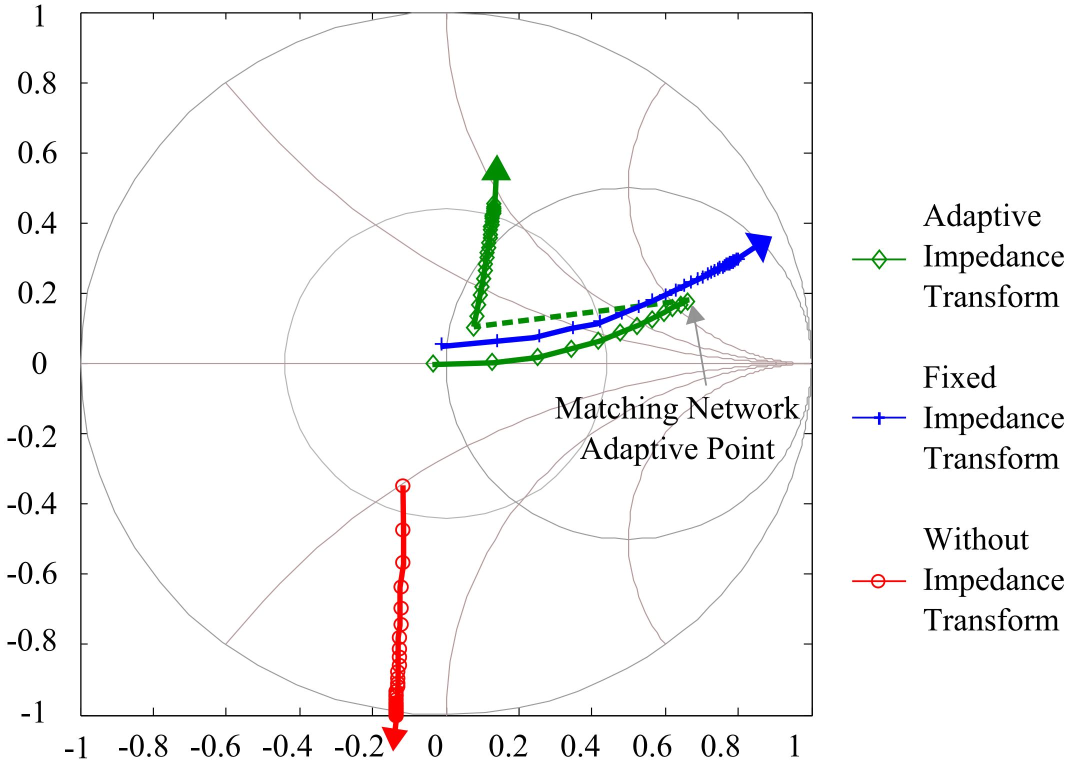


Fig. 5.16: Measured Input Impedance Over the Charging Process with Different Impedance Transform Circuitries

setup II has verified that with employing a static matching network which is designed according to the input impedance at the initial time point, both charging speed and output voltage are considerably improved. However, the functionality of the matching network fades due to the drift of the input impedance as the charging process proceeds. In setup III, the matching network works as a static one at the beginning as in setup II, and after a certain time, a control signal is applied to tune the matching network according to the input impedance of the rectifier obtained in setup I, in order to rematch the rectifier to the power source. The experiment has demonstrated the benefits of employing the adaptive matching network.

The theoretical charging procedure is predicted and depicted in Fig.5.17. To approach the theoretical performance of the charging procedure, the input impedance of the rectifier must be measured online continuously for determining the working status of the matching network of the next time slot, with the cost of the immense working load and design complexity of the feedback control circuitry.

5.5.1 Iterative Steepest Descent

To generate a feedback control signal, an iterative steepest descent approach functions theoretically by continuously sampling the current output voltage of the rectifier and based on the samples adaptively changing the control signal level. To implement such an

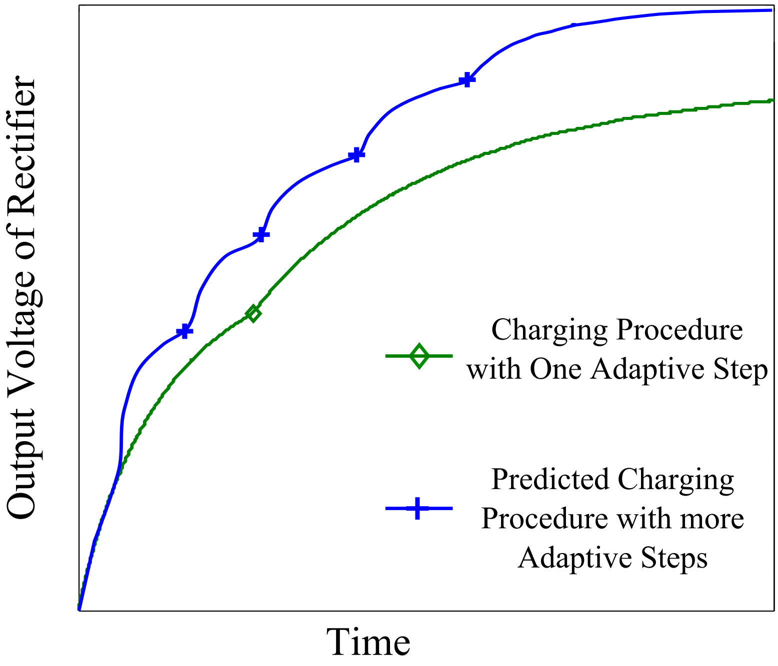


Fig. 5.17: Predicted Charging Procedure with More Adaptive Steps

algorithm, an ADC and a microcontroller are required, as shown in Fig.5.18.

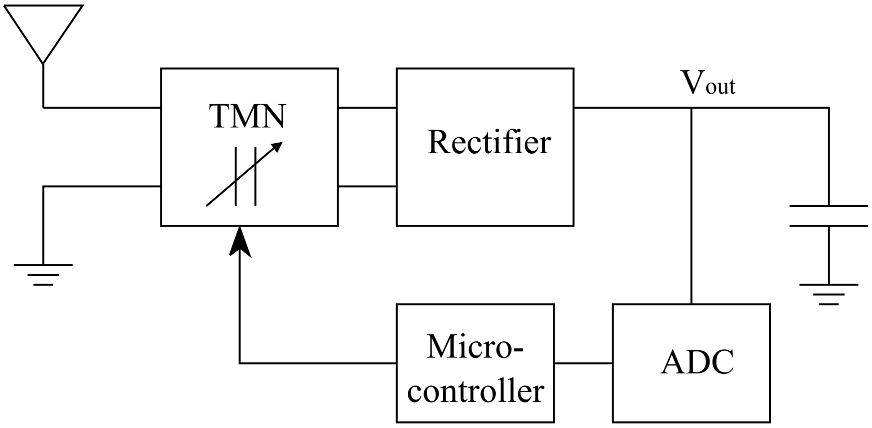


Fig. 5.18: Feedback Control with Iterative Steepest Descent Approach

5.5.2 Comparator-Based

In order to keep the circuitry less complex, a feedback control loop based on comparators is functional and more power-efficient. A reference voltage is determined based on the measurement of the input impedance of the rectifier over charging process. The output voltage of the rectifier is compared with the reference voltage in order to trigger the feedback control, as shown in Fig.5.19. In this approach, the matching network is tuned once the output voltage is larger than the reference voltage which improves the charging procedure for once as in setup III.

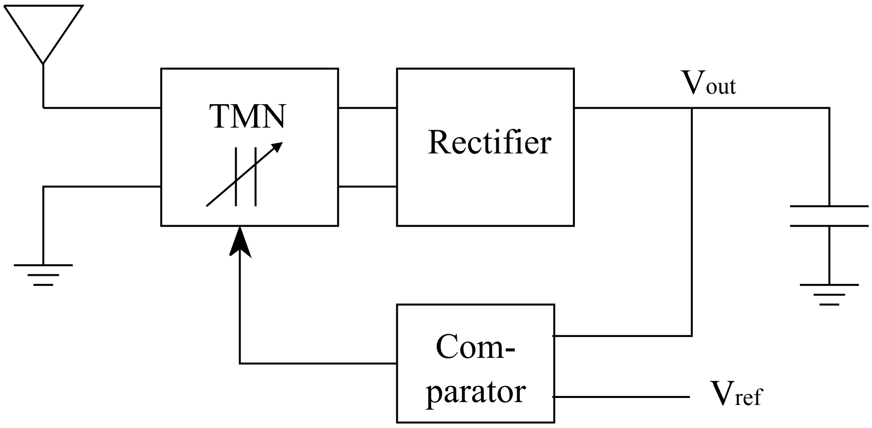


Fig. 5.19: Feedback Control Based on Comparator

5.5.3 Voltage Division

Both approaches proposed above are battery-based. The battery supplies power for the ADC, microcontroller and the reference voltage generator. In the case when battery is not available, the feedback control signal can be generated by the output voltage of the rectifier, as shown in Fig.5.21. The employment of a voltage divider is based on the nearly linear dependence between the output voltage and the desired C_M over charging procedure, as shown in Fig.5.20. To utilize the output voltage, a tuneable capacitor which

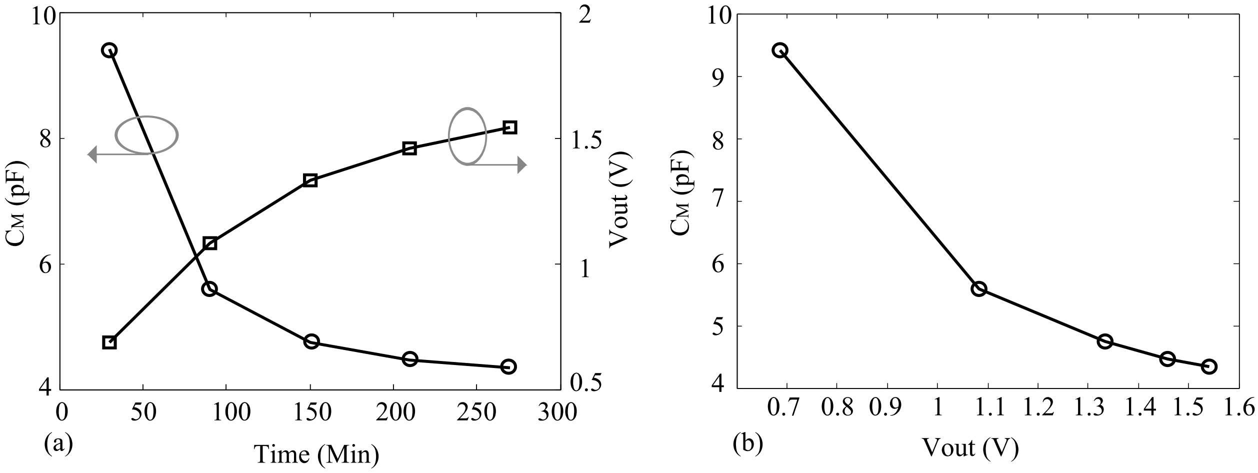


Fig. 5.20: (a) Change of Desired C_M and Output Voltage of Rectifier over Charging Procedure; (b) Nearly Linear Dependence between the Output Voltage and Desired C_M

operates in a very low voltage as well as low current consumption is preferred. For both battery-based approaches and non-battery-based approach where the control signal is generated by the output voltage of the rectifier, the adaptive control voltage level is a design challenge of the currently available tuneable capacitors based on MEMS, ferroelectric technologies.

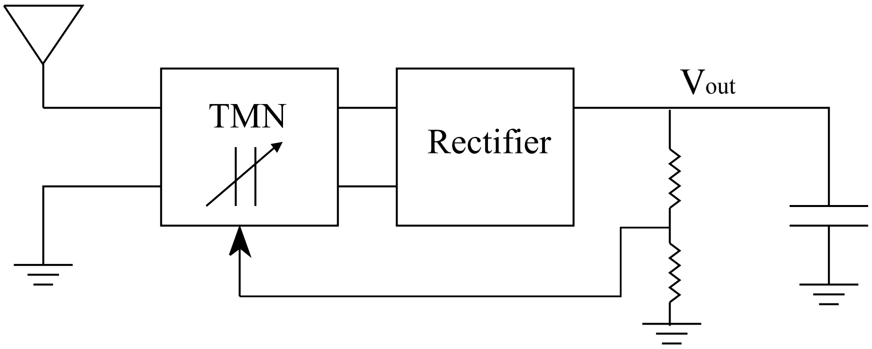


Fig. 5.21: Feedback Control Based on Output Voltage of Rectifier

5.6 Summary

In this chapter, the input impedance of a RF/DC rectifier is analyzed and observed during the charging phase, and based on the analysis, a technique is proposed to improve the charging speed of the RF/DC energy harvester by employing an adaptive matching network. The technique has been demonstrated with a prototype design by comparing with the current standard design methods. In the experimental setup, the proposed technique more than doubles the charging speed. The technique has been proposed for the objective application of wireless sensor nodes, and the further work would focus on the generating the feedback control signal based on the working status of the rectifier.

Chapter 6

Conclusions

Contents

This thesis has presented energy harvesting techniques for energy-autonomous electronic devices. Different energy transducers have been investigated and for each power management circuit is implemented. A hybrid energy harvesting system is developed to harvest electric power from the ambient solar and heat sources for the wireless sensor node application of bridge health monitoring. To improve the performance, different maximum power point tracking techniques have been explored. Further, energy harvesting from the radio frequency signal is emphasized aiming to improve the power transfer efficiency of the power management circuits.

6.1 Contributions of the Work

The contributions of this thesis can be summarized in the following points:

- System level analysis of integrated WSN with RFID reader is first done which denotes the importance of improving the power utilization to prolong the battery life. Methodology has been proposed to save the power by adaptively tuning the radiated power from the RFID reader according to the need of the transponders in different working phases. In the transponder design, the common employed energy harvesting circuit which consists of an antenna, a static matching network and a rectifier is suggested to be modified with adaptively tuning the matching network based on the current consumption of the transponder.
- The analysis of the RF-DC power harvester with dynamic loads has been focused and a new approach is investigated by adjusting the RF matching network accord-

ing to the operation conditions with the aid of a feedback control. A compact I/V model of diode-connected transistors working in strong-inversion and subthreshold is developed with the objective to simplify the analysis. Based on the model, the voltage sensitivity of the circuit is derived and analyzed. A load-dependent large-signal input resistance model and the minimum power required to achieve a certain DC voltage supply with variable load currents are then derived. The concept of an operation-controlled tuneable matching network is proposed in order to maximize the overall power efficiency.
Based on the theoretical analysis, a prototype implementation of a radio frequency wave energy harvester with the capability of self-adjusting the matching network to adapt to changing load conditions is realized. An auxiliary charge-pump is designed to supply the power for the supplemental control unit. The design is implemented in a standard 0.13-μm CMOS process. The prototype design is analysed based on its post-layout simulation. The results show that the power transfer efficiency with using the proposed design can achieve a level of over 70% independent of the load conditions, which indicates that the power transfer efficiency in variable operation states can be guaranteed with employing the autonomously adaptive matching network.

- Furthermore, the input impedance of a RF/DC rectifier is analyzed and observed during the charging phase, and based on the analysis, a technique is proposed to improve the charging speed of the RF/DC energy harvester by employing an adaptive matching network. The technique has been demonstrated with a prototype design by comparing with the current standard design methods. In the experimental setup, the proposed technique more than doubles the charging speed. The technique has been proposed for the objective application of wireless sensor nodes.

6.2 Directions for Future Work

The proposed methodology of employing an adaptively tuneable matching network in RF energy harvesting circuitry represents a novel perspective of improving the power utilization in remote wireless devices. It has also put forward new challenges to the tuneable devices operating in RF/microwave region. Some future work which can be focus on is summarized in the following points:

- To benefit the proposed methodology of improving the power utilization, a cognitive remote integrated WSN/RFID reader is to be developed which is able to radiate the wireless power adaptively according to the need of the passive devices.

- CMOS technology-based tuneable devices, like MOSFET switch, MOS varactors can be applied in low-voltage operation, but the power consumption is too high to be acceptable for tuneable matching network. Low-voltage, low-power-consumption tuneable devices like varactors are desired for the application in batteryless wireless devices.

- The feedback control circuit for adaptively tuning the matching network during the charging procedure has been studied. Proper topology is to be chosen for different application scenarios.
- Hybrid energy harvesting system design consisting of both ambient and dedicated energy sources is applicable for future wireless sensor networks to improve the reliability.

Appendix A

Modified Bessel Functions

A.1 Modified Bessel equation

$$x^2\frac{d^2y}{dx^2}+x\frac{dy}{dx}+((ix)^2-\nu^2)y=0 \tag{A.1}$$

where $i=\sqrt{-1}$, or equivalently:

$$x^2\frac{d^2y}{dx^2}+x\frac{dy}{dx}-(x^2+\nu^2)y=0 \tag{A.2}$$

For $x>0$, its solution is:

$$y=AJ_\nu(ix)+BY_\nu(ix) \tag{A.3}$$

or

$$y=CI_\nu(x)+DK_\nu(x) \tag{A.4}$$

where $I_\nu(x)$ and $K_\nu(x)$ are the modified Bessel functions of the first and second kind of order ν.

A.2 Modified Bessel Functions

Integral forms of modified Bessel functions for integer orders $n=0,1,2,3,...$

$$I_n(x)=\frac{1}{\pi}\int_0^\pi cos(n\theta)e^{(xcos\theta)}d\theta \tag{A.5}$$

with integer order $n=0$:

$$I_0(x)=\frac{1}{\pi}\int_0^\pi e^{(xcos\theta)}d\theta \tag{A.6}$$

Asymptotic approximation of modified Bessel functions:
for large values of x:

$$I_n(x)=\frac{e^x}{\sqrt{2\pi x}}[1-\frac{4n^2-1^2}{1(8x)}(1-\frac{4n^2-3^2}{2(8x)}(1-\frac{4n^2-5^2}{3(8x)}(1-...)))] \tag{A.7}$$

$$I_0(x) = \frac{e^x}{\sqrt{2\pi x}}[1 + \frac{1}{8x}(1 + \frac{9}{2(8x)}(1 + \frac{25}{3(8x)}(1 + ...)))] \tag{A.8}$$

References

[1] ADAPTIV ENERGY LLC. Building Blocks of an Energy Harvesting Solution. Technical Report AN003, 2009.

[2] I. F. AKYILDIZ, W. SU, Y. SANKARASUBRAMANIAM, and E. CAYIRCI. A Survey on Sensor Networks. *IEEE Communications Magazine*, 40:102–114, Aug. 2008.

[3] P. E. ALLEN and D. R. HOLBERG. *CMOS Analog Circuit Design*. Oxford University Press, 2002.

[4] P. ANDREANI and S. MATTISSON. On the Use of MOS Varactors in RF VCOs. *IEEE Journal of Solid-State Circuits*, 35(6):905–910, Jun. 2000.

[5] G. K. BALACHANDRAN and R. E. BARNETT. A 100nA Voltage Regulator System With Dynamic Bandwidth Boosting for RFID Systems. *IEEE Journal of Solid-State Circuits*, 41(9):2019–2028, Sept. 2006.

[6] R. BARNETT, S. LAZAR, and J. LIU. Design of Multistage Rectifiers with Low-Cost Impedance Matching for Passive RFID Tags. In *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pages 4–8, 2006.

[7] R. E. BARNETT, J. LIU, and S. LAZAR. A RF to DC Voltage Conversion Model for Multi-Stage Rectifiers in UHF RFID Transponders. *IEEE Journal of Solid-State Circuits*, 44(2):354–370, Feb. 2009.

[8] S. BEEBY and N. WHITE. *Energy Harvesting for Autonomous Systems*. Artech House, 2010.

[9] A. BELLAOUAR and M. I. ELMASRY. *Low-Power Digital VLSI Design Circuits and Systems*. Kluwer Academic Publishers, Massachusetts, 1995.

[10] E. BERGERET, J. GAUBERT, P. PANNIER, and J. M. GAULTIER. Modeling and Design of CMOS UHF Voltage Multiplier for RFID in an EEPROM Compatible Process. *IEEE Transactions on Circuit and Systems*, 54(10):833–837, Oct. 2007.

[11] D. BRUNELLI, C. MOSER, L. THIELE, and L. BENINI. Design of a Solar-Harvesting Circuit for Batteryless Embedded Systems. *IEEE Transactions on Circuit and Systems, I: Regular Papers*, 56(11):2519–2528, Nov. 2009.

[12] J. A. CHAVEZ, J. A. ORTEGA, J. SALAZAR, A. TURO, and M. J. GARCIA. SPICE Model of Thermoelectric Elements Including Thermal Effects . In *17th IEEE Instrumentation and Measurement Technology Conference, IMTC*, pages 1019–1023, 2000.

[13] P. CHEN, W. CHEN, C. WU, Y. TSENG, and C. HUANG. A Group Tour Guide System with RFIDs and Wireless Sensor Networks. In *6th international conference on Information processing in sensor networks*, pages 561–562, 2007.

[14] N. CHO, S. SONG, S. KIM, S. KIM, and H. YOO. A 5.1uW UHF RFID Tag Chip Integrated with Sensors for Wireless Environmental Monitoring. In *31st European Solid State Circuit Conference*, pages 279–282, 2005.

[15] C. C. CHU and C. L. CHEN. Robust Maximum Power Point Tracking Method for Photovoltaic Cells: A Sliding Mode Control Approach. *Solar Energy*, 83(8):1370–1378, Aug. 2009.

[16] J. CURTY, N. JOEHL, C. DEHOLLAIN, and M. J. DECLERCQ. Remotely Powered Addressable UHF RFID Integrated System. *IEEE Journal of Solid-State Circuits*, 40(11):2193–2202, Nov. 2005.

[17] J. P. CURTY, N. JOEHL, F. KRUMMENACHER, C. DEHOLLAIN, and M. J. DECLERQ. A Model for u-Power Rectifier Analysis and Design. *IEEE Transactions on Circuit and Systems, I: Regular Papers*, 52(12):2771–2778, Dec. 2005.

[18] S. DALOLA, M. FERRARI, V. FERRARI, M. GUIZZETTI, D. MARIOLI, and A. TARONI. Characterization of Thermoelectric Modules for Powering Autonomous Sensors. *IEEE Transactions on Instrumentation and Measurement*, 58(1):99–107, Jan. 2009.

[19] N. DE VICQ, F. ROBERT, J. PENDERS, B. GYSELINCKX, and T. TORFS. Wireless Body Area Network for Sleep Staging. In *Biomedical Circuits and Systems Conference (BIOCAS)*, pages 163–166, 2007.

[20] J. F. DICKSON. On-Chip High-Voltage Generation in Integrated Circuits Using an Improved Multiplier Technique. *IEEE Journal of Solid-State Circuits*, SC-11(3):374–378, Jun. 1976.

[21] A. DOLGOV, R. ZANE, and Z. POPOVIC. Power Management System for Online Low Power RF Energy Harvesting Optimization. *IEEE Transactions on Circuit and Systems*, 57(7):1802–1811, Jul. 2010.

[22] R. K. DRANEY. High Temperature Sensor for Bearing Health Monitoring. In *IEEE Aerospace Conference*, pages 1–7, 2008.

[23] Z. H. DUGHAISH. Lead Telluride As a Thermoelectric Material for Thermoelectric Power Generation. *Physica B: Condensed Matter*, 322(1-2):205–223, 2002.

[24] D. DUNWELL and B. FRANK. Accumulation-Mode MOS Varactors for RF CMOS Low-Noise Amplifiers. In *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pages 145–148, 2007.

[25] C. ENGLUND and H. WALLIN. RFID in Wireless Sensor Network. Technical report, Department of Signals and Systems, Chalmers University of Technology, 2004.

[26] EPCGLOBAL INC. *EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF Air Interface Protocol for Communications at 860MHz - 960MHz, Ver.1.2.0*, 2008.

[27] M. EROL-KANTARCI and H. T. MOUFTAH. Wireless Sensor Networks for Cost-Efficient Residential Energy Management in the Smart Grid. *IEEE Transactions on Smart Grid*, 2(2):314–325, Jun. 2011.

[28] T. ESRAM and P. L. CHAPMAN. Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques . *IEEE Transactions on Energy Conversion*, 22(2):439–449, Jun. 2007.

[29] EUROPEAN COMMISSION. *Energy Efficiency: Delivering the 20% target*, Nov. 2008.

[30] A. FACEN and A. BONI. CMOS power retriever for UHF RFID tags. *Electronics Letters*, 43(25):1424–1425, Dec. 2007.

[31] J. FALIN. Designing DC/DC converters based on SEPIC topology. *Analog Applications Journal*, 4Q:18–23, 2008.

[32] R. FALK, F. KOHLMAYER, A. KOPF, and M. LI. Mobile Multi-Purpose RFID System. In *3rd European Workshop on RFID Systems and Technologies (RFID SysTech)*, pages 1–8, 2007.

[33] T. FELDENGUT, R. KOKOZINSKI, and S. KOLNSBERG. A UHF Voltage Multiplier Circuit Using a Threshold-Voltage Cancellation Technique. In *PRIME PH.D. Research in Microelectronics and Electronics*, pages 288–291, 2009.

[34] N. FEMIA, G. PETRONE, G. SPAGNUOLO, and M. VITELLI. Optimization of Perturb and Observe Maximum Power Point Tracking Method. *IEEE Transactions on Power Electronics*, 20(4):963–973, Jul. 2005.

[35] K. FINKENZELLER. *RFID Handbook, Fundamentals and Applications in Contactless Smart Cards and Identification*. Wiley, New York, 1999.

[36] M. FLATSCHER, M. DIELACHER, J. PRAINSACK, R. MATISCHEK, T. HERNDL, T. LENTSCH, and W. PRIBYL. A bulk Acoustic Wave (baw)-Based Sensor Node for Automotive Wireless Sensor Networks. *Elektrotechnik und Informationstechnik*, 125(4):143–146, Apr. 2008.

[37] GAO RFID INC. Product Overview: The Jett - Rugged Handheld RFID Reader/Mobile Computer (243004), http://www.gaorfid.com.

[38] S. GEVORGIAN and A. VOROBIEV. Tuneable Metamaterials Based on Ferroelectric Varactors. In *37th European Microwave Conference*, pages 404–407, 2007.

[39] J. L. GONZLEZ, A. RUBIO, and F. MOLL. Human Powered Piezoelectric Batteries to Supply Power to Wearable Electronic Devices. *International journal of the Society of Materials Engineering for Resources*, 10(1):34–40, Mar. 2002.

[40] M. A. GREEN, K. EMERY, Y. HISHIKAWA, and W. WARTA. Solar cell efficiency tables (version 36). *Progress in Photovoltaics: Research and Applications*, 18:346–352, Jun. 2010.

[41] V. C. GUNGOR, B. LU, and G. P. HANCKE. Opportunities and Challenges of Wireless Sensor Networks in Smart Grid. *IEEE Transactions on Industrial Electronics*, 57(10):3557–3564, Oct. 2010.

[42] G. W. HART, H. M. BRANZ, and C. H. C. III. Experimental Tests of Open-Loop Maximum-Power-Point Tracking Techniques for Photovoltaic Arrays. *Solar Cells*, 13(2):185–195, Dec. 1984.

[43] N. S. HUDAKA and G. G. AMATUCCI. Small-scale energy harvesting through thermoelectric, vibration, and radiofrequency power conversion. *Journal of Applied Physics*, 103(101301):1–24, 2008.

[44] J. IHN and F. CHANG. Detection and Monitoring of Hidden Fatigue Crack Growth Using a Built-in Piezoelectric Sensor/Actuator Network: II. Validation Using Riveted Joints and Repair Patches. *Smart Materials and Structures*, 13(3):621–630, Jun. 2004.

[45] INFINEON TECHNOLOGIES. *Data Sheet: BB833-Silicon Tuning Diodes*, 2002.

[46] ISO/IEC. *International Standard: ISO/IEC 18000-6 Information Technology - Radio Frequency Identification for Item Management - Part 6: Parameters for Air Interface Communications at 860MHz to 960MHz*, first edition, 2004.

[47] ISO/IEC. *International Standard: ISO/IEC 18000-4 Information Technology - Radio Frequency Identification for Item Management - Part 4: Parameters for Air Interface Communications at 2.45GHz*, second edition, 2008.

[48] M. G. JABOORI, M. M. SAIED, and A. A. R. HANAFY. A Contribution to the Simulation and Design Optimization of Photovoltaic Systems. *IEEE Transactions on Energy Conversion*, 6(3):401–406, Sept. 1991.

[49] A. JAIN and A. KAPOOR. A new method to determine the diode ideality factor of real solar cell using Lambert W-function. *Solar Energy Materials & Solar Cells*, 85(3):391–396, Jan. 2005.

[50] S. JAIN and V. AGARWAL. A New Algorithm for Rapid Tracking of Approximate Maximum Power Point in Photovoltaic Systems. *IEEE Power Electronics Letters*, 2(1):16–19, Mar. 2004.

[51] Y. JIANG, Y. WANG, and K. CHOI. *Ferroelectrics - Material Aspects*, chapter BST and Other Ferroelectric Thin Films by CCVD and Their Properties and Applications, pages 3–30. InTech, 2011.

[52] U. KARTHAUS and M. FISCHER. Fully Integrated Passive UHF RFID Transponder IC With 16.7-uW Minimum RF Input Power. *IEEE Journal of Solid-State Circuits*, 38(10):1602–1608, Oct. 2003.

[53] A. KASYAP. Miniature Portable Ambient Energy Harvesting Modules Powered by RLP Technology: Joule-Thief. White paper, Adaptive Energy, Jun. 2009.

[54] M. KECK. A New Approach of a Piezoelectric Vibration-Based Power Generator to Supply Next Generation Tire Sensor Systems. In *IEEE Sensors*, pages 1299–1302, 2007.

[55] T.-Y. KIM, H.-G. AHN, S. K. PARK, and Y.-K. LEE. A Novel Maximum Power Point Tracking Control for Photovoltaic Power System Under Rapidly Changing Solar Radiation. In *IEEE International Symposium on Industrial Electronics, ISIE*, pages 1011–1014, 2001.

[56] M. KISHI, H. NEMOTO, T. HAMAO, M. YAMAMOTO, S. SUDOU, M. MANDAI, , and S. YAMAMOTO. Micro-Thermoelectric Modules and Their Application to Wristwatches as an Energy Source. In *18th International Conference on Thermoelectrics (ICT)*, pages 301–307, 1999.

[57] F. KOCER and M. P. FLYNN. A New Transponder ArchitectureWith On-Chip ADC for Long-Range Telemetry Applications. *IEEE Journal of Solid-State Circuits*, 41(5):1142–1148, May 2006.

[58] N. KONG, D. S. HA, A. ERTURK, and D. J. INMAN. Resistive Impedance Matching Circuit for Piezoelectric Energy Harvesting. *Journal of Intelligent Material Systems and Structures*, 21(13):1293–1302, Sept. 2010.

[59] K. KOTANI, A. SASAKI, and T. ITO. High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs. *IEEE Journal of Solid-State Circuits*, 44(11):3011–3018, Nov. 2009.

[60] E. KOUTROULIS, K. KALAITZAKIS, and N. C. VOULGARIS. Development of a Microcontroller-Based, Photovoltaic Maximum Power Point Tracking Control System. *IEEE Transactions on Power Electronics*, 16(1):46–54, Jan. 2001.

[61] Y.-C. KUO, T.-J. LIANG, and J.-F. CHEN. Novel Maximum-Power-Point-Tracking Controller for Photovoltaic Energy Conversion System. *IEEE Transactions on Industrial Electronics*, 48(3):594–601, Jun. 2001.

[62] J. KYMISSIS, C. KENDALL, J. PARADISO, and N. GERSHENFELD. Parasitic Power Harvesting in Shoes. In *Second International Symposium on Wearable Computing*, pages 132–139, 1998.

[63] T. H. LEE. *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2004.

[64] V. LEONOV, T. TORFS, P. FIORINI, and C. V. HOOF. Thermoelectric Converters of Human Warmth for Self-Powered Wireless Sensor Nodes. *IEEE Sensors Journal*, 7(5):650–657, May 2007.

[65] Y. LI, H. YU, B. SU, and Y. SHANG. Hybrid Micropower Source for Wireless Sensor Network. *IEEE Sensors Journal*, 8(6):678–681, Jun. 2008.

[66] H. LIU, M. BOLIC, A. NAYAK, and I. STOJMENOVIC. Taxonomy and Challenges of the Integration of RFID and Wireless Sensor Networks. *IEEE Network*, 22(6):26–32, Nov.-Dec. 2008.

[67] Y. LU, L. P. B. KATEHI, and D. PEROULIS. High-Power MEMS Varactors and Impedance Tuners for Millimeter-Wave Applications. *IEEE Transactions on Microwave Theory and Techniques*, 53(11):3672–3678, Nov. 2005.

[68] J. LYNCH and K. LOH. A Summary Review of Wireless Sensors and Sensor Networks for Structural Health Monitoring. *The Shock and Vibration Digest*, 38(2):91–128, Mar. 2006.

[69] J. P. LYNCH, A. SUNDARARAJAN, K. H. LAW, A. S. KIREMIDJIAN, T. KENNY, and E. CARRYER. Embedment of structural monitoring algorithms in a wireless sensing unit. *Structural Engineering and Mechanics*, 15(3):285–297, 2003.

[70] J. P. LYNCH, A. SUNDARARAJAN, K. H. LAW, H. SOHN, and C. R. FARRARC. Design of a Wireless Active Sensing Unit for Structural Health Monitoring. In *11th Annual International Symposium on Smart Structures and Materials*, pages 157–168, 2004.

[71] J. MAGET. *Varactors and Inductors for Integrated RF Circuits in Standard MOS Technologies*. PhD thesis, Universitaet Der Bundeswehr Muenchen, 2002.

[72] S. MANDAL and R. SARPESHKAR. Low-Power CMOS Rectifier Design for RFID Applications. *IEEE Transactions on Circuits and Systems*, 54(6):1177–1188, Jun. 2007.

[73] S. MANEEWAN and S. CHINDARUKSA. Thermoelectric Power Generation System Using Waste Heat from Biomass Drying. *Journal of Electronic Materials*, 38(7):974–980, 2009.

[74] M. A. S. MASOUM, H. DEHBONEI, and E. F. FUCHS. Theoretical and Experimental Analyses of Photovoltaic Systems With Voltage- and Current-Based Maximum Power-Point Tracking. *IEEE Transactions on Energy Conversion*, 4(4):514–522, Dec. 2002.

[75] R. MATTHEWS, N. J. MCDONALD, P. HERVIEUX, P. J. TURNER, and M. A. STEINDORF. A wearable physiological sensor suit for unobtrusive monitoring of physiological and cognitive state. In *29th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS)*, pages 5276–5281, 2007.

[76] F. MAZZILLI, P. E. THOPPAY, N. JOEHL, and C. DEHOLLAIN. Design Methodology and Comparison of Rectifiers for UHF-band RFIDs. In *IEEE Radio Frequency Integrated Circuits Symposium*, pages 505–508, 2010.

[77] MICROSEMI CORP. *Data Sheet: IGLOO Low-Power Flash FPGAs with Flash Freeze Technology, Rev. 21*, 2012.

[78] P. D. MITCHESON, E. M. YEATMAN, G. K. RAO, A. S. HOLMES, and T. C. GREEN. Energy Harvesting From Human and MachineMotion for Wireless Electronic Devices. *Proceedings of the IEEE*, 96(9):1457–1486, Sep. 2008.

[79] M. NARIMAN, R. ROFOUGARAN, and F. D. FLAVIIS. A Switched-Capacitor mm-Wave VCO in 65 nm Digital CMOS. In *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 157–160, 2010.

[80] G. K. OTTMAN, H. F. HOFMANN, A. C. BHATT, and G. A. LESIEUTRE. Adaptive Piezoelectric Energy Harvesting Circuit for Wireless Remote Power Supply. *IEEE Transactions on Power Electronics*, 17(5):669–676, Sep. 2002.

[81] T. PAING, J. SHIN, R. ZANE, and Z. POPOVIC. Resistor Emulation Approach to Low-Power RF Energy Harvesting. *IEEE Transactions on Power Electronics*, 23(3):1494–1501, May 2008.

[82] S. N. PAKZAD, G. L. FENVES, S. KIM, and D. E. CULLER. Design and Implementation of Scalable Wireless Sensor Network for Structural Monitoring. *Journal of Infrastructure Systems*, 14(1):89–101, Mar. 2008.

[83] G. PARK, H. H. CUDNEY, and D. J. INMAN. Impedance-Based Health Monitoring of Civil Structural Components. *Journal of Infrastructure Systems*, 6(4):153–160, Dec. 2000.

[84] J. PENDERS, B. GYSELINCKX, R. VULLERS, M. D. NIL, S. NIMMALA, J. VAN DE MOLENGRAFT, R. YAZICIOGLU, T. TORFS, V. LEONOV, P. MERKEN, and C. V. HOOF. Human++: From technology to emerging health monitoring concepts. In *5th International Workshop on Wearable and Implantable Body Sensor Networks*, pages 94–98, 2008.

[85] F. PHILIPP, F. A. SAMMAN, and M. GLESNER. Design of an Autonomous Platform for Distributed Sensing-Actuating Systems. In *22nd IEEE International Symposium on Rapid System Prototyping*, pages 85–90, 2011.

[86] PHYSIK INSTRUMENTE. *Data Sheet: DuraAct Piezoelectric Patch Transducer P-876*, 2008.

[87] PIEZOTAG LIMITED. Piezo Power Source for Tire Pressure Monitoring Systems. *Energy Harvesting Journal*, 2009.

[88] B. POUDEL, Q. HAO, Y. MA, Y. LAN, A. MINNICH, B. YU, Y. X, D. WANG, A. MUTO, D. VASHAEE, X. CHEN, J. LIU, M. S. DRESSELHAUS, G. CHEN, and Z. REN. High-Thermoelectric Performance of Nanostructured Bismuth Antimony Telluride Bulk Alloys. *Science*, 320(5876):634–638, May 2008.

[89] J. PROVOOST and R. V. SCHAIJK. IMEC Improves Piezoelectric Energy Harvesters to Drive Vehicle Health Monitoring. *Solid State Technology*, 8(4), Dec. 2008.

[90] H. RAMAMURTHY, B. S. PRABHU, R. GADH, and A. M. MADNI. Wireless Industrial Monitoring and Control using a Smart Sensor Platform. *IEEE Sensors Journal*, 7(5):611–618, Apr. 2007.

[91] S. ROBINET, B. GOMEZ, and N. DELORME. A CMOS-SOI 2.45GHz Remote-Powered Sensor Tag. In *IEEE International Solid-State Circuits Conference (ISSCC)*, pages 286–287; 614, 2008.

[92] F. D. ROSI. Thermoelectricity and Thermoelectric Power Generation. *Solid-State Electronics*, 11(9):833–868, Sep. 1968.

[93] S. ROUNDY. *Energy Scavenging for Wireless Sensor Nodes with a Focus on Vibration to Electricity Conversion*. PhD thesis, The University of California, Berkeley, 2003.

[94] S. ROUNDY and P. KWRIGHT. A piezoelectric vibration based generator for wireless electronics. *Smart Material and Structures*, 13(5):1131–1142, 2004.

[95] N. ROY, A. TRIVEDI, and J. WONG. Designing an FPGA-Based RFID Reader. *Xcell Journal*, Second Quarter(57):26–29, 2006.

[96] P. SAMENI, C. SIU, S. MIRABBASI, H. DJAHANSHAHI, M. HAMOUR, K. INIEWSKI, and J. CHANA. Modeling and Characterization of VCOs with MOS Varactors for RF Transceivers. *EURASIP Journal on Wireless Communications and Networking*, 2006:1–12, Aug. 2006.

[97] E. SANDOZ-ROSADO and R. J. STEVENS. Experimental Characterization of Thermoelectric Modules and Comparison with Theoretical Models for Power Generation. *Journal of Electronic Materials*, 38(7):1239–1244, 2009.

[98] E. SANDOZ-ROSADO and R. J. STEVENS. Robust Finite Element Model for the Design of Thermoelectric Modules. *Journal of Electronic Materials*, 39(9):1848–1855, 2010.

[99] S. SARMA and D. W. ENGELS. On the Future of RFID Tags and Protocols. Technical report, Auto-ID Center, Jun. 2003.

[100] P. SCHEELE, A. GIERE, Y. ZHENG, F. GOELDEN, and R. JAKOBY. Modeling and Applications of Ferroelectric-Thick Film Devices With Resistive Electrodes for Linearity Improvement and Tuning-Voltage Reduction. *IEEE Transactions on Microwave Theory and Techniques*, 55(2):383–390, Feb. 2007.

[101] L. SCHOR, P. SOMMER, and R. WATTENHOFER. Towards a Zero-Configuration Wireless Sensor Network Architecture for Smart Buildings. In *First ACM Workshop on Embedded Sensing Systems for Energy-Efficiency in Buildings*, pages 31–36, 2009.

[102] A. SHAMELI, A. SAFARIAN, A. ROFOUGARAN, M. ROFOUGARAN, and F. D. FLAVIIS. Power Harvester Design for Passive UHF RFID Tag Using a Voltage Boosting Technique. *IEEE Transactions on Microwave Theory and Techniques*, 55(6):1089–1097, Jun. 2007.

[103] N. SHENCK. A Demonstration of Useful Electric Energy Generation from Piezoceramics in a Shoe. Master's thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, 1999.

[104] N. S. SHENCK and J. A. PARADISO. Energy Scavenging With Shoe-Mounted Piezoelectrics. *IEEE Micro*, 21(3):30–42, May-Jun. 2001.

[105] V. SINGHVI, A. KRAUSE, C. GUESTRIN, J. H. G. JR., and H. S. MATTHEWS. Intelligent Light Control using Sensor Networks. In *3rd International Conference on Embedded Networked Sensor Systems*, pages 218–229, 2005.

[106] T. SOORAPANTH, C. P. YUE, D. K. SHAEFFER, T. H. LEE, and S. S. WONG. Analysis and Optimization of Accumulation-Mode Varactor for RF ICs. In *Symposium on VLSI Circuits Digest of Technical Papers*, pages 32–33, 1998.

[107] STACK LTD. *TPMS Pro Data Sheet: Battery-less Tyre Pressure & Temperature Monitoring System, Rev. 1.4*, 2012.

[108] G. SUBRAMANYAM, M. PATTERSON, K. LEEDY, R. NEIDHARD, C. VARANASI, C. ZHANG, and G. STEINHAUER. Linearity and Temperature Dependence of Large-Area Processed High-Q Barium Strontium Titanate Thin-film Varactors. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 57(7):1692–1695, Jul. 2010.

[109] J. TAVARES, F. J. VELEZ, and J. M. FERRO. Application of Wireless Sensor Networks to Automobiles. *Measurement Science Review*, 8(3):65–70, 2008.

[110] TEXAS INSTRUMENTS. CC253x System-on-Chip Solution for 2.4 GHz IEEE 802.15.4 and ZigBee Applications User's Guide. Technical report, Texas Instruments.

[111] THINGMAGIC INC. *Data Sheet MERCURY5e, http://www.thingmagic.com/embedded-rfid-readers/mercury5e*.

[112] B. TORRES, Q. PANG, G. W. SKELTON, S. BRIDGES, and N. MEGHANATHAN. Integration of an RFID to a Wireless Sensor Network and Its Use to Identify an Individual Carrying RFID Tags. *International Journal of Ad hoc, Sensor & Ubiquitous Computing (IJASUC)*, 1(4):1–15, Dec. 2010.

[113] UC BERKELEY. *BSIM3v3.2.2 MOSFET Model Users's Manual*, 1999.

[114] T. UMEDA, H. YOSHIDA, S. SEKINE, Y. FUJITA, T. SUZUKI, and S. OTAKA. A 950-MHz Rectifier Circuit for Sensor Network Tags With 10-m Distance. *IEEE Journal of Solid-State Circuits*, 41(1):35–41, Jan. 2006.

[115] M. VEERACHARY, T. SENJYU, and K. UEZATO. Maximum Power Point Tracking Control of IDB Converter Supplied PV System. *IEE Proceedings Electric Power Applications*, 148(6):494–502, Nov. 2001.

[116] J. VICTORY, Z. YAN, G. G. ANDC. MCANDREW, and J. ZHENG. A Physically Based, Scalable MOS Varactor Model and Extraction Methodology for RF Applications. *IEEE Transactions on Electron Devices*, 52(7):1343–1352, Jul. 2005.

[117] C. B. VINING. An Inconvenient Truth About Thermoelectrics. *Nature Materials*, 8:83–85, Feb. 2009.

[118] H. J. VISSER, A. C. F. RENIERS, and J. A. C. THEEUWES. Ambient RF Energy Scavenging: GSM and WLAN Power Density Measurements. In *38th European Microwave Conference (EuMC)*, pages 721–724, 2008.

[119] G. D. VITA and G. IANNACCONE. Design Criteria for the RF Section of UHF and Microwave Passive RFID Transponders. *IEEE Transactions on Microwave Theory and Techniques*, 53(9):2978–2990, Sep. 2005.

[120] R.-J. M. VULLERS, R. SCHAIJK, H.-J. VISSER, J. PENDERS, and C. HOOF. Energy Harvesting for Autonomous Wireless Sensor Networks. *IEEE Solid-State Circuits Magazine*, 2(2):29–38, 2010.

[121] M. WAGNER. *Simulation of Thermoelectric Devices*. PhD thesis, Technischen Universitaet Wien , 2007.

[122] C. WATKINS, B. SHEN, and R. VENKATASUBRAMANIAN. Low-Grade-Heat Energy Harvesting Using Superlattice Thermoelectrics for Applications In Implantable Medical Devices and Sensors. In *24th International Conference on Thermoelectrics (ICT)*, pages 265–267, 2005.

[123] S. WONG and C. CHEN. Power Efficient Multi-stage CMOS Rectifier Design for UHF RFID Tags. *Integration, the VLSI Journal*, 44(3):242–255, Jun. 2011.

[124] W. XIAO and W. G. DUNFORD. A Modified Adaptive Hill Climbing MPPT Method for Photovoltaic Power Systems. In *35th Annual IEEE Power Electronics Specialists Conference*, volume 3, pages 1957–1963, 2004.

[125] L. YEH, Y. WANG, and Y. TSENG. iPower: an energy conservation system for intelligent buildings by wireless sensor networks. *International Journal of Sensor Networks*, 5(1):1–10, Feb. 2009.

[126] J. YI, W.-H. KI, and C.-Y. TSUI. Analysis and Design Strategy of UHF Micro-Power CMOS Rectifier for Micro-Sensor and RFID Applications. *IEEE Transactions on Circuit and Systems, I: Regular Papers*, 54(1):153–166, Jan. 2007.

[127] R. YORK, A. NAGRA, E. ERKER, T. TAYLOR, P. PERIASWAMY, J. SPECK, S. STREIFFER, and O. AUCIELLO. Microwave integrated circuits using thin-film BST . In *12th IEEE International Symposium on Applications of Ferroelectrics*, volume 1, 195-200, 2000.

[128] G. J. YU, Y. S. JUNG, J. Y. CHOI, and G. S. KIM. A Novel Two-Mode MPPT Control Algorithm Based on Comparative Study of Existing Algorithms. *Solar Energy*, 76(4):455–463, Apr. 2004.

[129] H. YU, Y. LI, Y. SHANG, and B. SU. Design and Investigation of Photovoltaic and Thermoelectric Hybrid Power Source for Wireless Sensor Networks. In *3rd IEEE Int. Conf. on Nano/Micro Engineered and Molecular Systems*, pages 196–201, 2008.

[130] L. ZHANG and Z. WANG. Integration of RFID into Wireless Sensor Networks: Architectures, Opportunities and Challenging Problems. In *Fifth International Conference on Grid and Cooperative Computing Workshops (GCCW)*, pages 463–469, 2006.

[131] P. ZHAO, T. HOLLSTEIN, and M. GLESNER. Analysis on Power Harvesting Circuit with Tunable Matching Network for Improved Efficiency. In *PRIME PH.D. Research in Microelectronics and Electronics*, pages 96–99, 2009.

[132] Y. ZHENG, A. HRISTOV, A. GIERE, and R. JAKOBY. Suppression of Harmonic Radiation of Tunable Planar Inverted-F Antenna by Ferroelectric Varactor Loading. In *IEEE MTT-S International Microwave Symposium*, pages 959–962, 2008.

[133] X. ZHU. *Switchable and Tunable Ferroelectric Thin Film Radio Frequency Components*. PhD thesis, University of Michigan, 2009.

[134] Z. ZHU, B. JAMALI, and P. H. COLE. Brief Comparison of Different rectifier structures for HF and UHF RFID (Phase II). Auto-ID Labs, 2004.

List of Publications

[135] F. Philipp, P. Zhao, F. A. Samman, and M. Glesner. Monitoring and Control of a Dynamically Reconfigurable Wireless Sensor Node Powered by Hybrid Energy Harvesting. In *University Booth at Design, Automation & Test in Europe (DATE), Hardware Demonstration*, 2011.

[136] F. Philipp, P. Zhao, F. A. Samman, M. Glesner, K. B. Dassanayake, S. Maheswararajah, and S. Halgamuge. Adaptive Wireless Sensor Networks Powered by Hybrid Energy Harvesting for Environmental Monitoring. In *International Conference on Information and Automation for Sustainability, ICIAfS*, 2012.

[137] O. Soffke, P. Zhao, T. Hollstein, and M. G. . Modelling of HF and UHF RFID Technology for System and Circuit Level Simulations. In *3rd European Workshop on RFID Systems and Technologies (RFID-SysTech), VDE-Verlag, ISBN 978-3-8007-3045-2*, pages 1–6, June 2007.

[138] P. Zhao and M. Glesner. RF Energy Harvester Design with Autonomously Adaptive Impedance Matching Network Based on Auxiliary Charge-Pump Rectifier. In *IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 2477–2480, 2011.

[139] P. Zhao, T. Hollstein, and M. Glesner. Analysis on Power Harvesting Circuit with Tunable Matching Network for Improved Efficiency. In *PRIME PH.D. Research in Microelectronics and Electronics*, pages 96–99, 2009.

[140] P. Zhao, Y. Zheng, and M. Glesner. Automatic Impedance Matching in Microwave Power Harvesters. In *PRIME PH.D. Research in Microelectronics and Electronics*, pages 1–4, 2010.

[141] P. Zhao, Y. Zheng, T. Hollstein, K. Fang, R. Jakoby, and M. Glesner. A Novel Software Defined Radio Architecture with Automatic Power Control for RFID Readers. In *IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS)*, pages 1–6, Nov. 2009.

[142] P. Zhao, Y. Zheng, T. Hollstein, R. Jakoby, and M. Glesner. Real-Time Operation-Based Power Consumption Analysis for Passive UHF RFID Transponders. In *Proc. of 54th International Wissenschaftliches Kolloquium (IWK)*, September 2009.

Supervised Theses

[143] L. Cui. Study and development of reconfigurable RF frontend for RFID reader. Master Thesis, 01.07.2010-28.02.2011.

[144] K. Fang. Investigation of Software Defined Radio Architecture and Power Control Algorithm for Multiprotocol RFID Readers. Diplomarbeit, 01.05.2009-01.11.2009.

[145] M. Fasil. Development of reconfigurable local oscillator for RFID reader. Studienarbeit, 01.07.2010-30.09.2010.

[146] J. Mai. Research and Design on Energy Harvesting with TEG. Student Internship for Graduate Study, 15.10.2010 to 15.01.2011.

[147] X. Song. Implementation,Synthesize,Dynamic Power Estimation of UHF RFID Transponders. Master Thesis, 01.11.2009-30.05.2010.

[148] J. Zhang. Design and Implement Piezoelectric MEMS Energy Harvesting Circuit. Student Internship for Graduate Study, 15.10.2010 - 30.03.2011.

[149] Z. Zhong. Analytical Model Development of UHF Micro-Power Rectifiers for RFID Applications. Studienarbeit, 16.06.2008-15.09.2008.

Lebenslauf

Ping Zhao

Zur Person:

Geburtsdatum:	06. Dez. 1983
Geburtsort:	Shandong, China

Ausbildung:

1997 bis 2000	Gymnasium in Shandong Abschluss: Abitur
2000 bis 2004	Studentin an der Fakultät für Informatik, Wissenschaft und Engineering, Shandong University Abschluss: Bacheloringenieur
2003 bis 2004	Studentin an der Fakultät für Ingenieurwissenschaften und Informatik, Universität Ulm Austausch-Studium
2004 bis 2007	Studentin an der Fakultät für Elektronik, Nachrichtentechnik und Informationstechnik, Technische Universität Darmstadt Abschluss: Masteringenieur
seit dem 1.7.2007	Doktorandin am Fachgebiet Mikroelektronische Systeme der Technischen Universität Darmstadt

Beruflicher Werdegang:

07.2006 bis 12.2006	Praktikantin an der Firma Diehl Aerospace GmbH in Frankfurt am Main.
seit dem 1.7.2007	Wissenschaftliche Mitarbeiterin am Fachgebiet Mikroelektronische Systeme der Technischen Universität Darmstadt